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No. 6405R

# JVC Service Manual

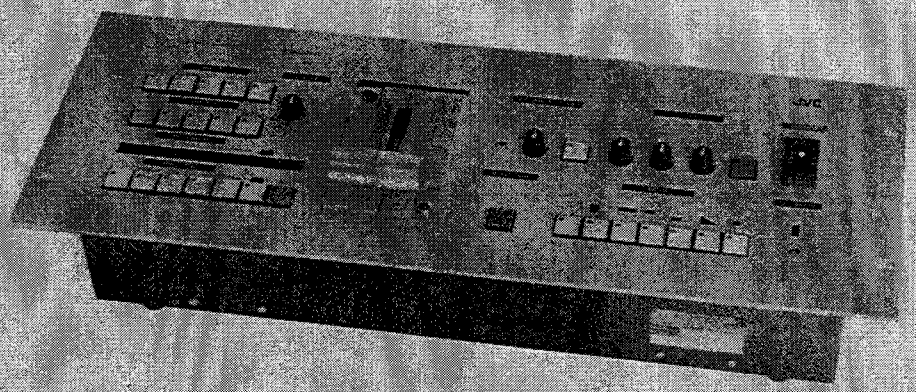
## COLOUR SPECIAL EFFECTS GENERATOR

## MODEL KM-1200

VICTOR COMPANY OF JAPAN, LIMITED

No. 6405R

# JVC Service Manual



MODEL KM-1200

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# Important Safety Precautions

Prior to shipment from the factory, JVC products are strictly inspected to conform with the recognized product safety and electrical codes of the countries in which they are to be sold. However, in order to maintain such compliance, it is equally important to implement the following precautions when a set is being serviced.

## ● Precautions during Servicing

1. Locations requiring special caution are denoted by labels and inscriptions on the cabinet, chassis and certain parts of the product. When performing service, be sure to read and comply with these and other cautionary notices appearing in the operation and service manuals.

2. Parts identified by the ⚠ symbol and shaded (▒) parts are critical for safety.
   Replace only with specified part numbers.
   **Note: Parts in this category also include those specified to comply with X-ray emission standards for products using cathode ray tubes and those specified for compliance with various regulations regarding spurious radiation emission.**

3. Fuse replacement caution notice.
   Caution for continued protection against fire hazard.
   Replace only with same type and rated fuse(s) as specified.

4. Use specified internal wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads

5. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulation Tape
   2) PVC tubing
   3) Spacers
   4) Insulation sheets for transistors
   5) Barrier

6. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.) wrap ends of wires securely about the terminals before soldering.

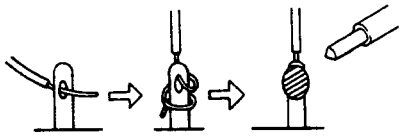


Fig. 1

7. Observe that wires do not contact heat producing parts (heat-sinks, oxide metal film resistors, fusible resistors, etc.)

8. Check that replaced wires do not contact sharp edged or pointed parts.

9. When a power cord has been replaced, check that 10—15 kg of force in any direction will not loosen it.

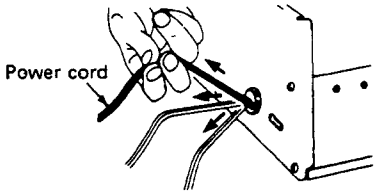



Fig. 2

10. Also check areas surrounding repaired locations.

11. Products using cathode ray tubes (CRTs)
    In regard to such products, the cathode ray tubes themselves, the high voltage circuits, and related circuits are specified for compliance with recognized codes pertaining to X-ray emission. Consequently, when servicing these products, replace the cathode ray tubes and other parts with only the specified parts. Under no circumstances attempt to modify these circuits. Unauthorized modification can increase the high voltage value and cause X-ray emission from the cathode ray tube.

12. Crimp type wire connector
    In such cases as when replacing the power transformer in sets where the connections between the power cord and power transformer primary lead wires are performed using crimp type connectors, if replacing the connectors is unavoidable, in order to prevent safety hazards, perform carefully and precisely according to the following steps.

    1) **Connector part number** : E03830-001
    2) **Required tool** : Connector crimping tool of the proper type which will not damage insulated parts.
    3) **Replacement procedure**
       (1) Remove the old connector by cutting the wires at a point close to the connector.
       Important : Do not reuse a connector (discard it).

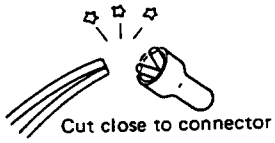



Fig. 3

(2) Strip about 15 mm of the insulation from the ends of the wires. If the wires are stranded, twist the strands to avoid frayed conductors.

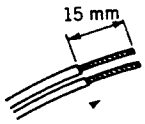



Fig. 4

(3) Align the lengths of the wires to be connected. Insert the wires fully into the connector.

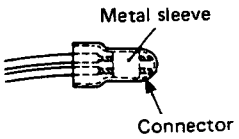



Fig. 5

(4) As shown in Fig. 6, use the crimping tool to crimp the metal sleeve at the center position. Be sure to crimp fully to the complete closure of the tool.

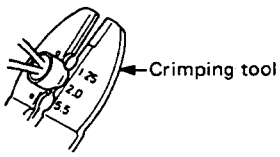



Fig. 6

(5) Check the four points noted in Fig. 7.

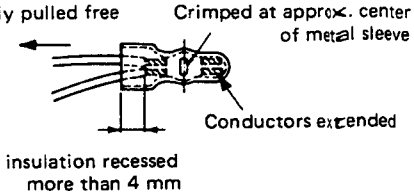

Not easily pulled free
Crimped at approx. center of metal sleeve
Conductors extended
Wire insulation recessed more than 4 mm

Fig. 7

## ● Safety Check after Servicing

Examine the area surrounding the repaired location for damage or deterioration. Observe that screws, parts and wires have been returned to original positions, Afterwards, perform the following tests and confirm the specified values in order to verify compliance with safety standards.

1. **Insulation resistance test**
   Confirm the specified insulation resistance or greater between power cord plug prongs and externally exposed parts of the set (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.). See table 1 below.

2. **Dielectric strength test**
   Confirm specified dielectric strength or greater between power cord plug prongs and exposed accessible parts of the set (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.). See table 1 below.

3. **Clearance distance**
   When replacing primary circuit components, confirm specified clearance distance (d), (d') between soldered terminals, and between terminals and surrounding metallic parts. See table 1 below.

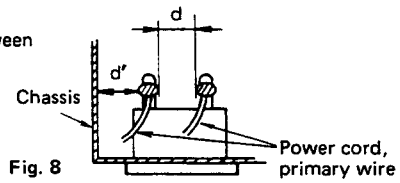


Fig. 8

4. **Leakage current test**
   Confirm specified or lower leakage current between earth ground/power cord plug prongs and externally exposed accessible parts (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.).
   **Measuring Method:** (Power ON)
   Insert load Z between earth ground/power cord plug prongs and externally exposed accessible parts.
   Use an AC voltmeter to measure across both terminals of load Z. See figure 9 and following table 2.

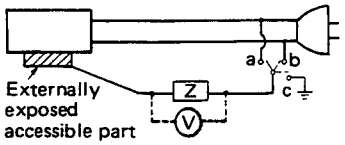


Fig. 9

5. **Grounding (Class I model only)**
   Confirm specified or lower grounding impedance between earth pin in AC inlet and externally exposed accessible parts (Video in, Video out, Audio in, Audio out or Fixing screw etc.).
   **Measuring Method:**
   Connect milli ohm meter between earth pin in AC inlet and exposed accessible parts. See figure 10 and grounding specifications.

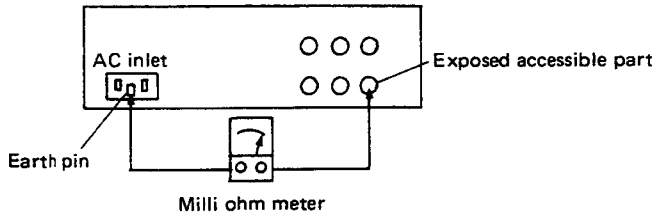


Fig. 10

**Grounding Specifications**

| Region | Grounding Impedance (Z) |
|---|---|
| USA & Canada | Z ≦ 0.1 ohm |
| Europe & Australia | Z ≦ 0.5 ohm |

| AC Line Voltage | Region | Insulation Resistance (R) | Dielectric Strength | Clearance Distance (d), (d') |
|---|---|---|---|---|
| 100 V | Japan | R≧1 MΩ/500 V DC | AC 1 kV 1 minute | d, d' ≧ 3 mm |
| 100 to 240 V | | | AC 1.5 kV 1 minute | d, d' ≧ 4 mm |
| 110 to 130 V | USA & Canada | – | AC 900 V 1 minute | d, d' ≧ 3.2 mm |
| 110 to 130 V<br>200 to 240 V | Europe & Australia | R≧10 MΩ /500 V DC | AC 3 kV 1 minute (Class II)<br>AC 1.5 kV 1 minute (Class I) | d ≧ 4 mm<br>d' ≧ 8 mm (Power cord)<br>d' ≧ 6 mm (Primary wire) |

**Table 1** Specifications for each region

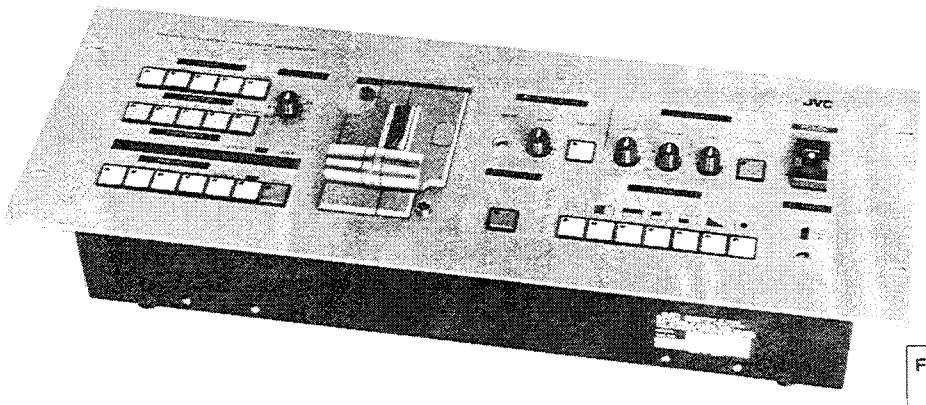
| AC Line Voltage | Region | Load Z | Leakage Current (i) | a, b, c |
|---|---|---|---|---|
| 100 V | Japan | 1 kΩ | i ≦ 1 mA rms | Exposed accessible parts |
| 110 to 130 V | USA & Canada | 0.15 μF, 1.5 kΩ | i ≦ 0.5 mA rms | Exposed accessible parts |
| 110 to 130 V<br>220 to 240 V | Europe & Australia | 2 kΩ | i ≦ 0.7 mA peak<br>i ≦ 2 mA dc | Antenna earth terminals |
| | | 50 kΩ | i ≦ 0.7 mA peak<br>i ≦ 2 mA dc | Other terminals |

**Table 2** Leakage current specifications for each region

**Note:** These tables are unofficial and for reference only. Be sure to confirm the precise values for your particular country and locality.

# JVC Instructions

# COLOR SPECIAL EFFECTS GENERATOR
# KM-1200




**For Customer Use:**

Enter below the Serial No. which is located on the bottom of the cabinet. Retain this information for future reference.

Model No. KM-1200

Serial No. _____

Due to design modifications, the servicing procedures and data given in this manual are subject to possible change without prior notice.

**WARNING:**

**TO PREVENT FIRE OR SHOCK HAZARD, DO NOT EXPOSE THIS APPLIANCE TO RAIN OR MOISTURE.**

**AVERTISSEMENT:**

**POUR EVITER LES RISQUES D'INCENDIE OU D'ELECTROCUTION, NE PAS EXPOSER L'APPAREIL A L'HUMIDITE OU A LA PLUIE.**

**Warning Notice**
**FOR YOUR SAFETY**

To ensure safe operation the three-pin plug supplied must be inserted only into a standard three-pin power point which is effectively grounded through the normal household wiring.
Extension cords used with the equipment must be three-core and be correctly wired to provide connection to earth ground. Wrongly wired extension cords are a major cause of fatalities.
The face that the equipment operates satisfactorily does not imply that the power point is properly grounded and that the installation is completely safe. For your safety, if in any doubt about the correct grounding of the power point, consult a qualified electrician.

CAUTION
RISK OF ELECTRIC SHOCK
DO NOT OPEN
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK,
DO NOT REMOVE COVER (OR BACK).
NO USER-SERVICEABLE PARTS INSIDE.
REFER SERVICING TO QUALIFIED SERVICE PERSONNEL.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

Thank you for purchasing the KM-1200 Color Special Effects Generator. To gain maximum benefit from its use, it is suggested that you read these instructions carefully. After reading it, retain this booklet for future reference.

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# 1. FEATURES

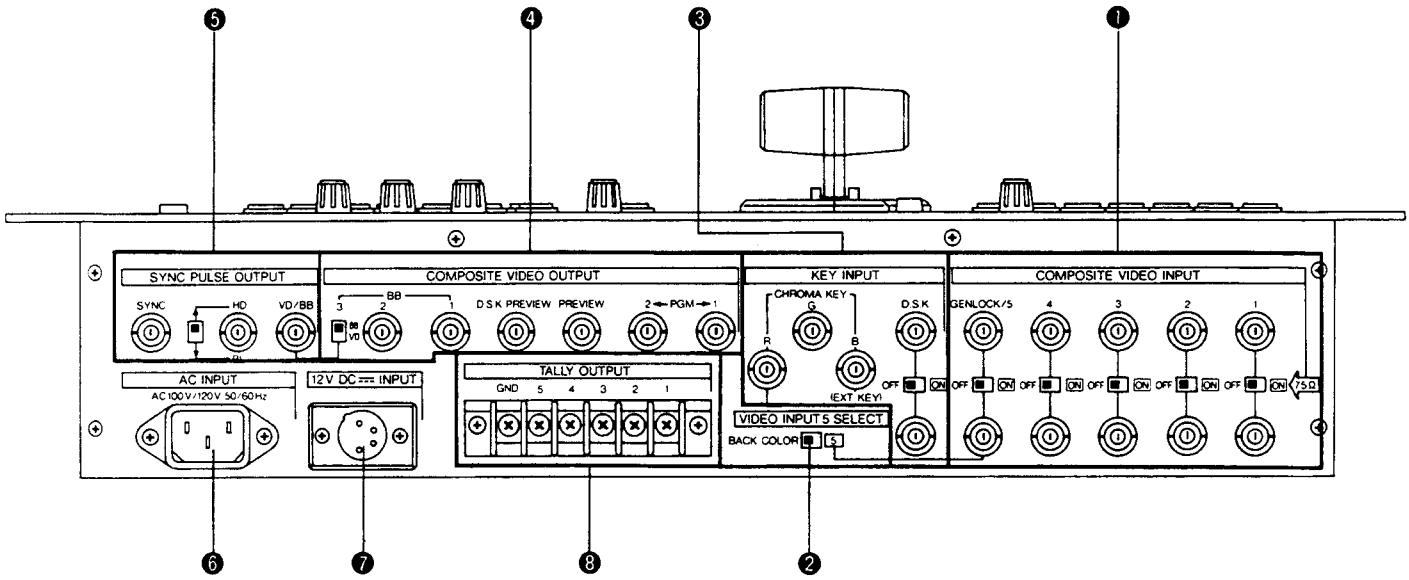
- **Chroma key generator built in**
  The built-in RGB chroma key generator enables chroma effects without using any external equipment. However, external keying is also possible via one of the Chroma Key Input terminals.
- **Downstream keyer built in**
- **Wipe effects**
  6 wipe effects are built in.
- **Auto-take function**
  An AUTO TAKE switch is provided so cut-in of desired picture on the preview monitor is possible.
- **Color background generator built in**
- **Vertical interval switching system**
- **DSK preview output terminal**
- **Built-in SSG with genlock function**
- **DC (11 to 17 V) operation possible**

# 2. PRECAUTIONS

- For an extended service life, avoid using the unit in a place subject to extreme temperatures, high humidity, strong vibrations, excessive dust, or in a place near the source of noise.
- Avoid strong vibrations and shocks when installing or carrying.
- Do not apply strong force to the fader lever or handle it violently.
- The standard positioning of the control panel is horizontal. Never lean it by more than 45° from the horizontal.
- When RS-2000/RS-1900/RS-110/RS-500 remote control units are used together in a system centered around the KM-1200, set the tally control mode of all units to "voltage supply". (See page 9)
- When the KM-1200 is mounted in an AV console or rack, leave a 1-unit space above the control panel for rear panel connections.

# 3. CONTROLS, CONNECTORS AND INDICATORS

## Rear Panel




**❶ COMPOSITE VIDEO INPUT connectors**

Inputs 1 – 4: BNC connectors with bridged connection. When not bridge-connected, set the 75 Ω termination switch to "ON".

GENLOCK/5: For genlock operation, input composite video (VBS) or black burst (BB) signal to this connector.
When there is no signal input to this connector, the synchronizing mode is set to internal mode (INT MODE) using the built-in SSG.

**❷ VIDEO INPUT 5 SELECT switch**

When the input to GENLOCK/5 connector ❶ is used for genlock and when all the input connectors 1 to 4 have already been used, the GENLOCK/5 input can be used as the fifth video input signal by setting this switch to "5". Consequently, a color background cannot be used.
However, when the input to the GENLOCK/5 connector is off, the fifth input reverts to the background color even if this switch is set to "5".

**❸ KEYING SIGNAL INPUT connectors**

DSK: Video signal input for downstream keying.

CHROMA KEY: Video signal inputs for chroma keying. (R/G/B signals without sync)

(EXT. KEY): Video signal input for external keying.

**Note:**

- **Among the above keying functions, chroma keying and external keying cannot be performed at the same time.**

**❹ COMPOSITE VIDEO OUTPUT connectors**

PGM 1, PGM 2: Program video output connectors.

PREVIEW: Preview video output connector.

DSK PREVIEW: DSK preview output connector. By monitoring this output, the settings (slice and color levels) of the downstream keyer can be checked without inserting it in the program line.

BB-1, BB-2: Outputs of black burst* signal.

BB-3: When the BB/VD switch is set to "BB", the black burst signal is output from VD/BB output connector ❺.

*Black burst signal: A composite signal consisting of sync and burst signals.

**❺ SYNC PULSE OUTPUT connectors**

75 Ω output connectors for HD, VD. SYNC and BL signals. Used for the genlock of a B & W camera for DSK or EXT keying.

SYNC: Sync signal output.

HD/BL: HD or BL signal output selectable by the switch.

VD/BB: The signal (VD or BB) selected by the BB-3 select switch of ❹ is output.

**❻ AC INPUT**

Connect the AC power cable provided.

**❼ DC INPUT**

XLR-type 4-pin connector for operating the unit with a 12 V DC power supply.

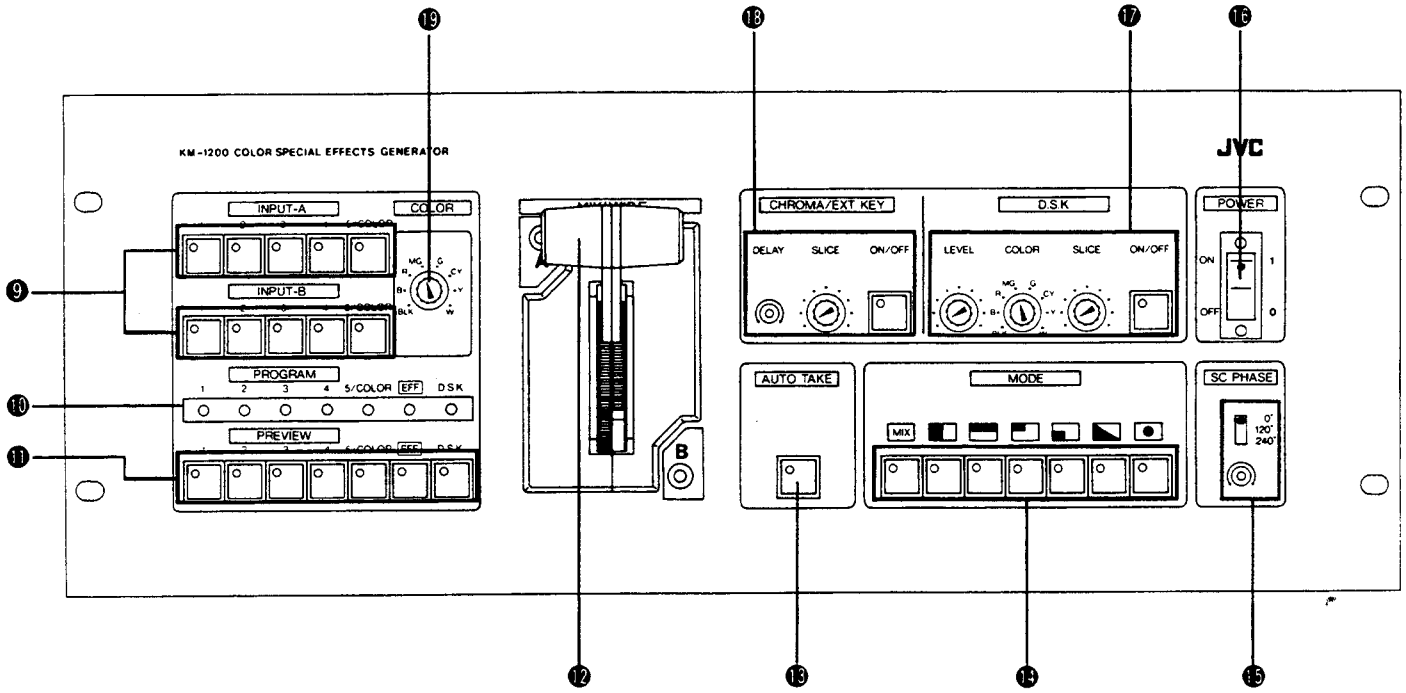
**Notes:**

- The DC power used should have a rated capacity of more than 1.5 A.

**❽ TALLY connectors**

The tally system uses the power supply method (with 5 V DC output) and the power is supplied through these terminals.

## Control Panel




**❾ INPUT-A and INPUT-B bus lines**
Select the bus lines to be input to the effects circuit (MIX/WIPE) among 5 video signals, which include 4 composite video inputs and the signal selected by VIDEO INPUT 5 SELECT switch ❷ (background color or genlock signal). When a button is pressed, the lamp lights indicating the selection of the input.

**❿ PROGRAM OUTPUT indicators**
The light indicates the signal output via the PGM output connectors ❹.

**⓫ PREVIEW bus line**
One of the 5 video inputs, effects circuit output signal (PGM) or DSK signal can be selected without it entering the program line, and output via PREVIEW output connector ❹.

**⓬ MIX/WIPE lever**
The lever varies the amount of mixing (of the video signals selected by the INPUT-A and INPUT-B bus lines) when MODE select switch ⓭ is set for "MIX", and controls wiping when the switch is set for a wipe pattern.

**⓭ AUTO TAKE button**
When this button is pressed, the video signal selected for the PREVIEW bus line is output as the PGM output. Auto-take is not possible for the DSK signal.

**⓮ MODE select buttons**
Selects the operation of the effects circuit, among mixing and 6 wipe patterns as shown below.

**⓯ SUBCARRIER PHASE control**
When the genlock signal is used as one of the images, the hue can be fine adjusted by this control.

**⓰ POWER switch**

**⓱ DOWNSTREAM KEYER controls**
Control the keying of the effects circuit output signal using the DSK video signal input.
ON/OFF: DSK signal output ON/OFF button.
SLICE: Adjusts the slice level of the DSK input signal.
COLOR: The color with which keying signal is generated is selected by this 8-position switch: BLK (black), B (blue), R (red), MG (magenta), G (green), CY (cyan), Y (yellow) and W (white).
LEVEL: Adjusts the DSK signal output level.

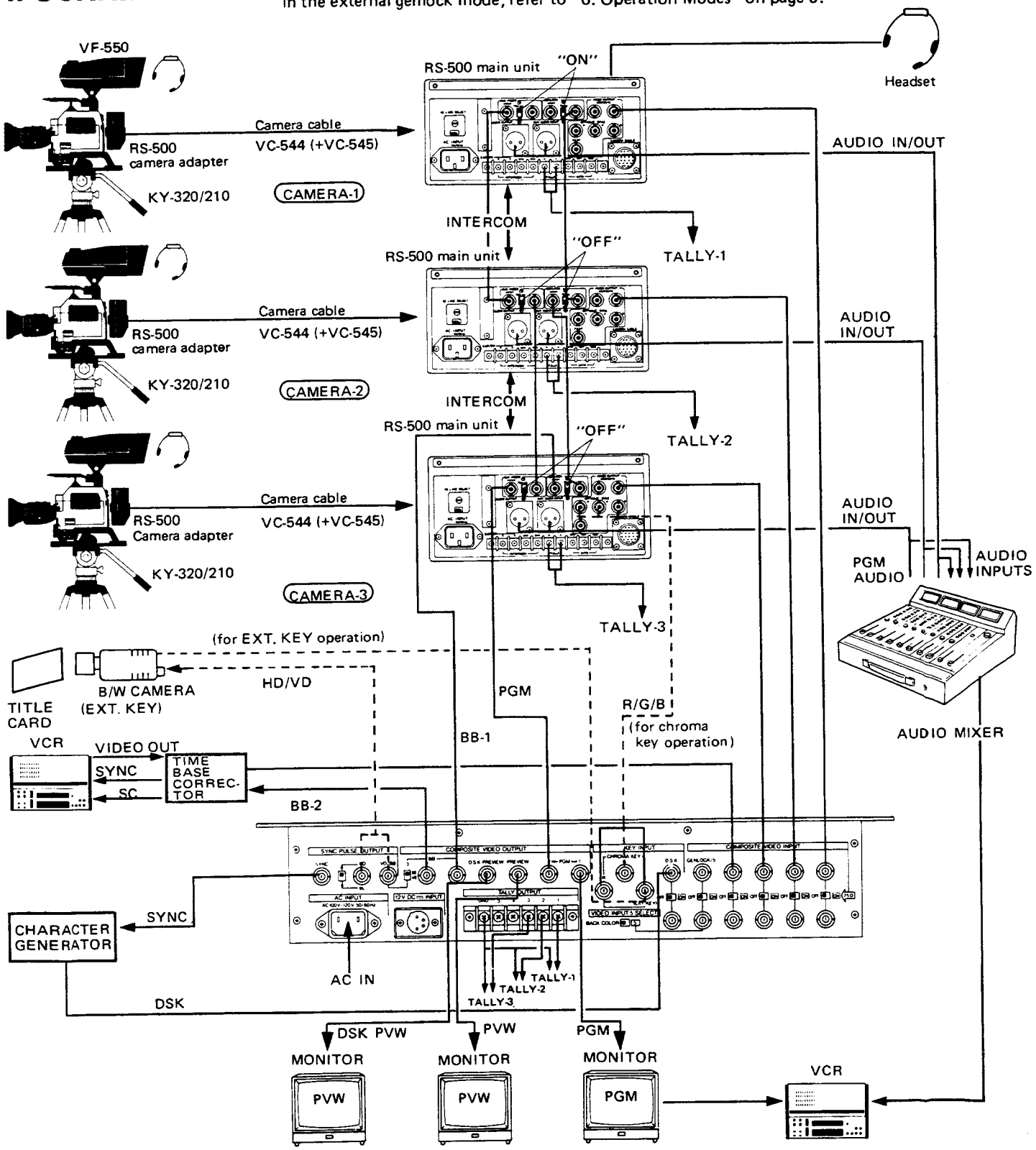
**⓲ CHROMA KEY controls**
ON/OFF: Keying signal ON/OFF button.
SLICE: Adjusts the most natural position of keying effect.
DELAY: When there is a delay between the key camera's main line signal (VBS) and chroma keying input signal, adjust using this potentiometer.

**⓳ COLOR (background color) selector**
Color background generation is a special effect with which the background of the picture is made a solid color. The signal from the color background generator is supplied to "5/COLOR" of each bus line. This switch is used to select one of 8 background colors; BLK (black), B (blue), R (red), MG (magenta), G (green), CY (cyan), Y (yellow) and W (white).

**Note:**
- The color background function cannot be used when the genlock signal is used as the 5th picture signal.

# 4. CONNECTIONS

This example shows an application of the unit in the internal sync mode. To operate the unit in the external genlock mode, refer to "6. Operation Modes" on page 9.




– Set the 75 Ω termination switches of all the input connectors which are not connected to "ON". –

**Notes:**

- For the connection and operation of the color video cameras, remote control units and video recorders shown in the diagram, refer to the instructions provided with them.
- Chroma and external keying cannot be performed at the same time.
- Video recorder playback signals contain a large amount of jitter (variations of time periods between sync signals) and dropout. For special effects using these signals, we recommend the use of a TBC (timebase corrector).

# 5. OPERATIONS

## 5.1 System Adjustment

**After making connections, it is necessary to perform this "system adjustment" as the signal levels and phases are not matched between the individual units making up the system.**
Only a simplified adjustment procedure is described here. The adjustment is more precise when a vectorscope and waveform monitor are connected to the output.

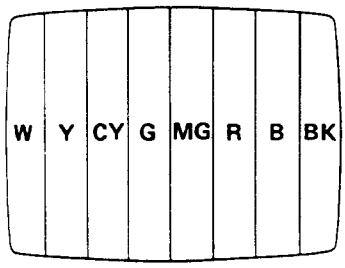
[1] Turn on all units in the system.
When power is switched on, the KM-1200 is automatically set for A bus line "1", B bus line "1", PREVIEW bus line "1", MODE "MIX", and PROGRAM "1".

[2] Set the BARS switches of the connected color video cameras to "ON" to generate color bar signals.

[3] Set the controls on the KM-1200 as follows:
- Set the MIX/WIPE lever to "A".
- Set the DSK ON/OFF button to "OFF" and turn the DSK LEVEL and DSK SLICE controls counterclockwise.
- Set the CHROMA KEY ON/OFF button to "OFF"

[4] Switch the PREVIEW bus-line buttons and monitor the preview monitor to check that the color bars signals from the cameras are input.
- Check that the 75 Ω termination switches of the input connectors are set to "ON". (Terminate also unused input connectors.)

[5] Adjust the horizontal phase and subcarrier phase.
1) Press the INPUT A and PREVEW buttons "1".
2) Press the AUTO TAKE button.
3) Press the PREVIEW buttons "1" and "DSK" alternately. At this time, adjust the H PHASE control of the camera connected to "1" so that the picture is not shifted to the left or right on the preview monitor screen.
Similarly, adjust the SC PHASE controls on the cameras so that the hues of color bars from different cameras are the same.




[6] Perform these adjustments for all the cameras connected.

[7] Shoot the same object (gray scale, etc.) with all cameras, and fine-adjust the black level (pedestal level), white level (video level) and chroma level, etc.

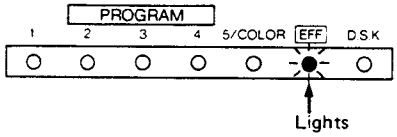
**Note:**
- For the operation of the color video cameras and remote control units, refer to the instructions provided with them.
- For EXT. genlock operation, subcarrier phase adjustment is necessary. Refer to the second item in "7. Operation Modes".

## 5.2 Primary Functions

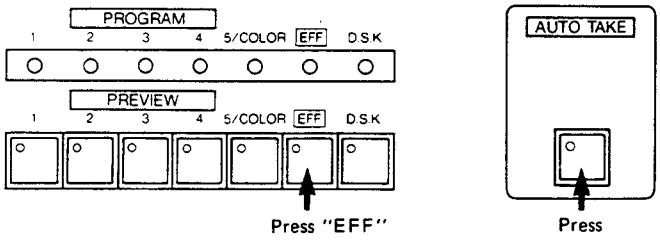
**Before operation, connect as shown in "4. Connections" and perform "5.1 System adjustment".**

**1. Picture selection**

1) Switching
1 Set the MIX/WIPE lever to "A".
2 Confirm that the "EFF" LED of the PROGRAM OUTPUT indicators is lit (indicating that the effects output signal is selected for the program output).



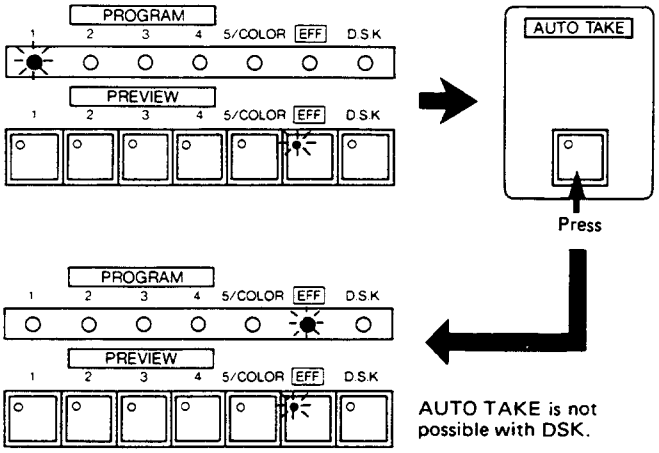

When a different LED is lit, press PREVIEW bus-line button "EFF" then press the AUTO TAKE button.
The "EFF" LED lights with this operation.




3 Press the required button of the INPUT A bus line. The selected signal is output as the PGM output.

**Note:**
- The same operation can be performed with the B bus line when the MIX/WIPE lever is set to "B".

2) Auto-take
Press one of the PREVIEW bus-line buttons selecting the picture on the preview monitor, then press the AUTO TAKE button. The image is output at the PGM output and the tally of the auto-take camera lights.

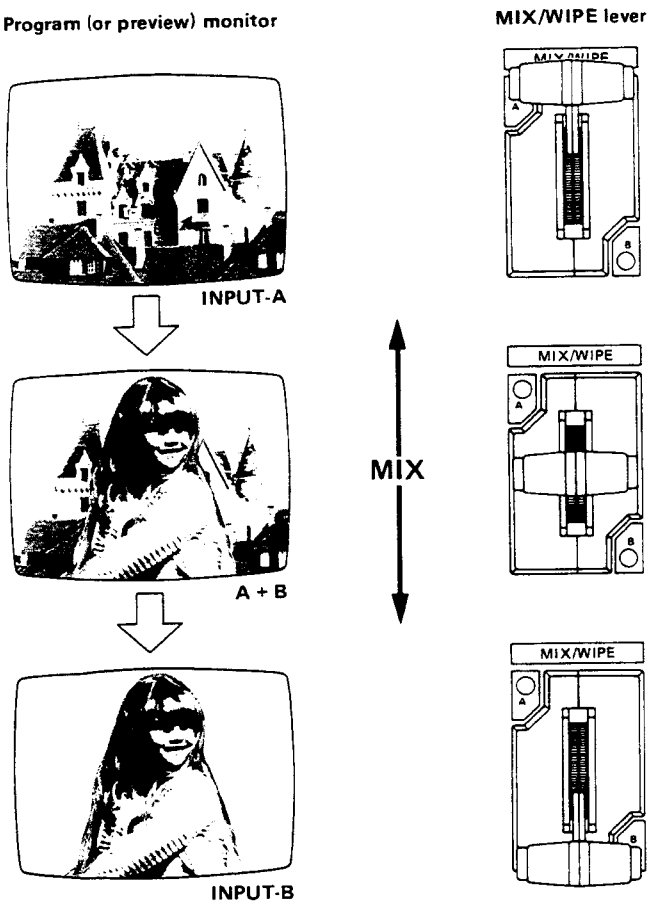


## 2. MIX operation

The INPUT-A and INPUT-B pictures can be mixed by following the procedure below. The MIX function enables image switching in which the A bus line picture gradually fades while the B bus line picture gradually appears (overlapped or dissolved).

- The effect signal is output at the PGM output using the auto-take operation. (The PROGRAM "EFF" LED lights.)
- Move the MIX/WIPE lever fully to "A".
- Press the required INPUT-A button.

[1] Set the MODE selector buttons to "MIX".
[2] Press the required INPUT-B button.
[3] Slide the MIX/WIPE lever to "B".
The pictures of A and B bus lines are mixed until the output picture is completely changed to the B bus line picture.



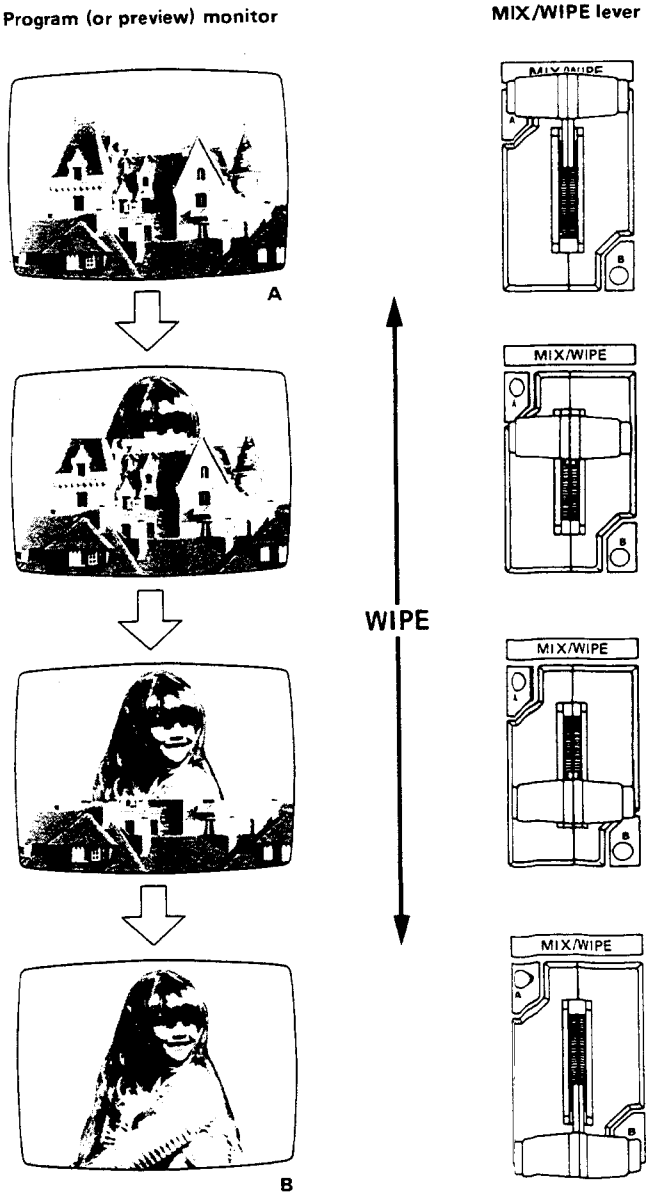

## 3. WIPE operation

Change between the INPUT-A and INPUT-B pictures is possible by wiping them vertically and horizontally.

- The effect signal is output at the PGM output using the AUTO TAKE button. (The PROGRAM "EFF" LED lights.)
- Slide the MIX/WIPE lever fully to "A".
- Press the required INPUT-A bus-line button.

[1] Press the required wipe pattern button. (For example, ▬)
[2] Press the required INPUT-B bus-line button.
[3] Slide the MIX/WIPE lever to "B".
The INPUT-A picture is wiped and finally replaced by the INPUT-B picture.

- The effect varies depending on the wipe pattern:
Before using this effect, confirm the effect on the preview monitor.



## 5.3 Secondary Functions

### 1. Color Background

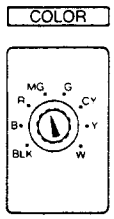
With the color background generation function, a solid color image filling the screen is generated purely electronically without using a camera, and this can be used as one of pictures handled by the KM-1200.

The COLOR switch on the control panel allows the selection of one of the eight colors: BLK (black), B (blue), R (red), MG (magenta), G (green), CY (cyan), Y (yellow) and W (white).

By selecting the 5/COLOR button of each bus line, the color picture selected can be used as the 5th input.

Note:

- **In the Ext. Genlock mode in which genlock signal is used as the 5th picture image, the color background function cannot be used.**



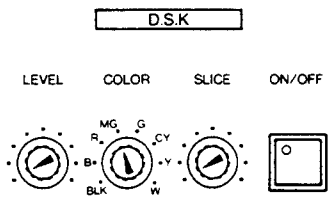

### 2. DSK (Downstream Keyer)

With this function, character or graphic images shot by a B/W camera can be added to the EFF output. These monochrome characters and graphics can be provided with a color by using the colorizer function.

- Connect a color monitor to DSK PREVIEW or PREVIEW OUTPUT, and press the PREVIEW bus-line button "DSK".
- To the DSK input connector, supply signal from a B/W camera or character generator.

[1] Adjust the SLICE and LEVEL controls so that color picture is observed on the DSK PREVIEW or PREVIEW monitor.

[2] Set the required color using the DSK COLOR switch.




[3] Set the DSK button to "ON" so that the DSK signal is inserted in the PGM output.

Note:

- When the characters and graphics inserted with DSK have high color saturation, dots may be observed at the edges because of the interference of color subcarriers. This is due to the operating principle of color TV itself and is not a malfunction.

### 3. Keying (CHROMA KEY/EXT KEY)

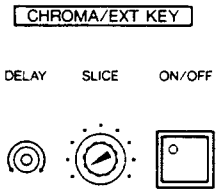
The KM-1200 incorporates a chroma key signal generator so, by supplying R/G/B signals to the CHROMA KEY INPUT R/G/B connectors, **chroma keying is possible with a blue background.**

When video signal (positive polarity) of characters or graphics shot by a B/W camera such as a title camera is input to the CHROMA KEY INPUT B connector, keying of A and B bus-line pictures is possible using that signal.

**Chroma keying and Ext. keying cannot be performed at the same time.**

1) Chroma keying operation

- Set the MODE select button to "MIX".
- Supply the video signal from the color camera for chroma keying (hereafter referred to as key camera) to one of the COMPOSITE VIDEO INPUT connectors.
- Set the CHROMA KEY ON/OFF button to "OFF".



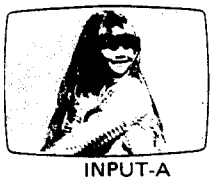

[1] Set the PREVIEW bus-line button to "EFF".

[2] Slide the MIX/WIPE lever to "A".

[3] Press the INPUT-A bus-line button corresponding to the input from the key camera.

[4] With the key camera, shoot the desired object using a blue background.

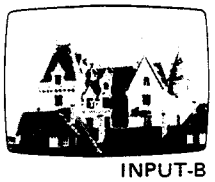
Blue background



INPUT-A
(Key camera)

[5] Slide the MIX/WIPE lever to "B".

[6] Press the INPUT-B bus-line button corresponding to the picture that you want to insert over the blue background shot by the key camera.

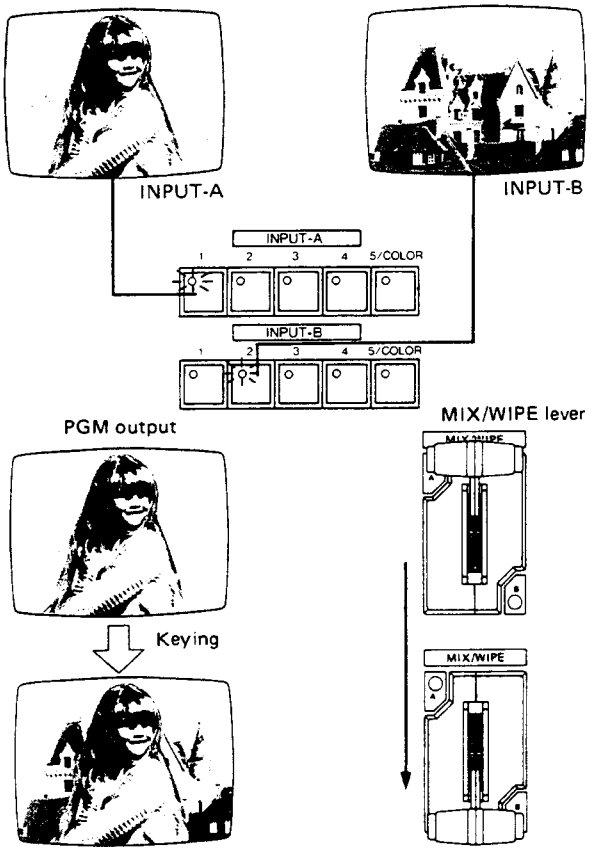


INPUT-B

[7] Set the CHROMA KEY ON/OFF button to "ON".
Adjust the SLICE control so that clear picture is observed on the preview monitor.

[8] Adjust the DELAY potentiometer so that the contours of the inserted picture are clear.

9 Slide the MIX/WIPE lever to "A".
10 Press the AUTO TAKE button.
(The EFF signal is output as the program output, which is, in the case, the signal from the key camera.)
11 Slide the MIX/WIPE lever slowly to "B": Only the blue part of the key camera picture is replaced by the B bus line picture.



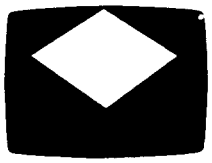

- To use the chroma keying effect as cut switching, follow the procedure below instead of above procedures 9 to 11 ;
  1) Slide the MIX/WIPE lever to "B".
  2) Press the AUTO TAKE button.
- When a wipe pattern button is pressed instead of the MODE "MIX" button, you can obtain a superimposed effect by shifting the MIX/WIPE lever.
- By reversing the selections of the INPUT-A and INPUT-B bus-line buttons (when the key camera signal is selected for the B bus-line), the key camera's blue part remains while the A bus-line picture replaces the other parts.

**Notes:**

- The blue part should be as deep as possible so that the blue can be replaced by the picture correctly.
- The illumination of the object being shot should be uniform.
- Usually the DELAY potentiometer does not have be adjusted once it has been set.
- Chroma keying may not be clearly distinguished if the focus of the key camera is not correct.

2) External keying operation

- Supply the video signal (positive polarity) from the video camera for external keying (hereafter referred to as EXT key camera) to the CHROMA KEY B input connector.
  For keying operation in which the B/W EXT key camera picture is black letters/images on a white background (negative polarity), connect the camera signal to the CHROMA KEY R or G input connector.
- Set the MODE select button to " MIX ".
- Set the CHROMA KEY ON/OFF button to "OFF".



(Example)
EXT KEY camera

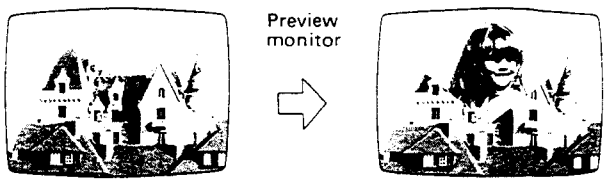
1 Set the PREVIEW bus-line button to "EFF".
2 Slide the MIX/WIPE lever to "A".
3 Press the INPUT-A bus-line button of the desired picture.

INPUT-A

4 Slide the MIX/WIPE lever to "B".
5 Press the INPUT-B bus-line button of the picture you want to insert.

INPUT-B

6 Set the CHROMA KEY ON/OFF button to "ON". Adjust the SLICE control so that clear picture is observed on the preview monitor.




7 Slide the MIX/WIPE lever to "A".
8 Press the AUTO TAKE switch.
(The EFF signal is output as the program output, which is in this case the A bus line signal.)
9 Slide the MIX/WIPE lever slowly to "B" to perform the keying effect.

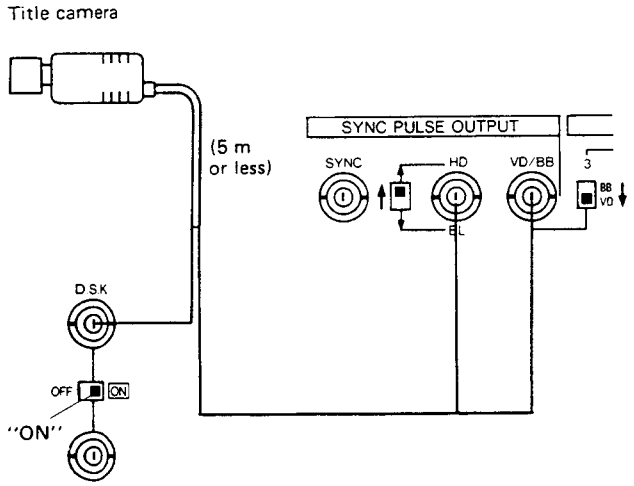
**4. Title Camera Drive Signal (SYNC PULSE OUTPUT)**

The title camera used for DSK or EXT keying should be genlocked with the sync system of the KM-1200.

The sync signal for title camera is supplied from the SYNC PULSE OUTPUT connector. The HD, VD, SYNC or BL signal can be selected according to the camera used.

The length of the cable between the KM-1200 and the camera for DSK should be within 5 m or 16.5 ft (5 m for sync supply cable and 5 m for return video cable, 10 m or 32.5 ft in total).

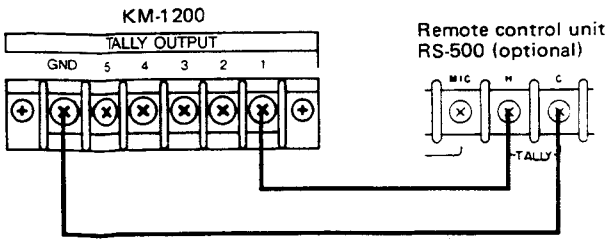
When the cable is too long, the H phase may become different when the preview monitor is switched between DSK and EFF.




# 6. TALLY CONNECTION

In a video system using more than one camera, it is necessary to indicate the camera operators and actors which cameras are on-the-air. This function is performed by the tally signal.

- Connect the TALLY connector on the rear panel to the Tally terminal of the other equipment (for example the optional RS-500) as shown below.
  The KM-1200 supplies 5 V DC to the system.




Operate tally within the following ratings to other equipments.

Voltage supply: 5 V DC, 1 mA max.

# 7. OPERATION MODES

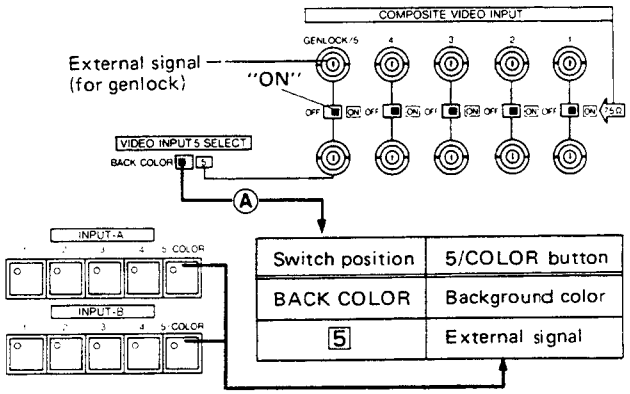
The KM-1200 can operate on either of the following two genlock modes as described below.

**1) INT mode**

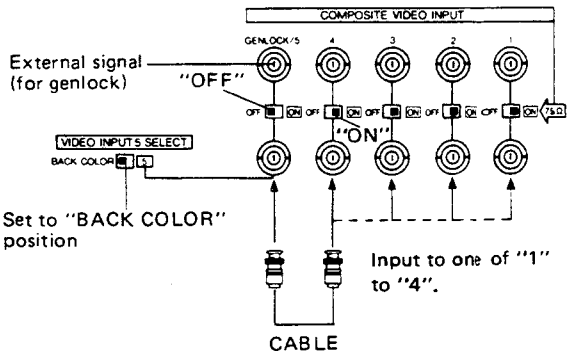
The whole system is synchronized with the internal SSG. The connection and operation methods in these instructions describe this mode.

**2) EXT genlock mode**

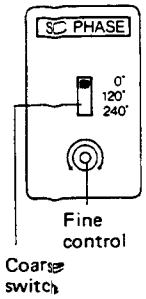
The whole system is synchronized by external composite video signal (VBS) or black burst (BB) signal.




- As shown above, the external signal connected to the GENLOCK/5 connector becomes the genlock reference signal.
  When switch Ⓐ is set to "5", the external signal can be used as the 5th picture input for each bus-line. When switch Ⓐ is set to "BACK COLOR", the external signal can be used only as the genlock reference signal while the color background function becomes available for each bus lines. (Simultaneous use is not possible.)
- To use the EXT genlock reference signal at the same time for the color background function, use the loop through connection as shown below.

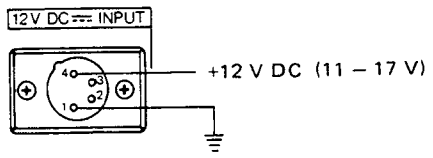



- When using the external signal as the 5th picture input, it is necessary to adjust the SC phase by the following procedure.
  1. Press the INPUT-A and PREVIEW bus-line switches corresponding to the external signal input.
  2. Slide the MIX/WIPE lever to "A".
  3. Adjust the SC PHASE switch and potentiometer so that the hues displayed on the preview monitor are the same when the PREVIEW bus line is alternately switched between "DSK" and the external signal input.



# 8. DC POWER SUPPLY

The KM-1200 can also operate on a DC power supply, by connecting 12 V DC to the XLR 4-pin connector on the rear panel. The rated output of the DC power supply used must have a capacity of more than 1.5 A.




# 9. SPECIFICATIONS

**Input Signals**

Video inputs : 5, composite video signals, 1.0 Vp-p (75 Ω or high impedance looped-through output), termination switch provided (4 inputs in INT mode or when color background function is used in EXT GENLOCK mode)

Chroma key input : R/G/B non-composite or composite video signal, 1.0 Vp-p (with SYNC) or 0.7 Vp-p (without SYNC)

(EXTERNAL key input) : 1, composite or non-composite video signal, 1.0 Vp-p (with SYNC) or 0.7 Vp-p (without SYNC), (Chroma key and EXT key operations cannot be performed simultaneously.)

(DSK input) : 1, composite or non-composite video signal, 1.0 Vp-p (with SYNC) or 0.7 Vp-p (without SYNC) (75 Ω or high impedance looped-through output), termination switch provided

Genlock input : 1, composite video signal 1.0 Vp-p or black burst 0.43 Vp-p (NTSC)/ 0.45 Vp-p (PAL) (75 Ω or high impedance looped-through output), termination switch provided

**Output Signals**

Program output : 2, composite video signal 1.0 Vp-p, 75 Ω (BNC)

Preview output : 1, composite video signal 1.0 Vp-p, 75 Ω (BNC)

DSK preview output : 1, composite video signal 1.0 Vp-p, 75 Ω (BNC)

Synchronization output : HD, VD and SYNC, BL 4.0 Vp-p, 75 Ω (BNC)

BB1, BB2, BB3 } Black burst, 0.43 Vp-p (NTSC) 0.45 Vp-p (PAL), 75 Ω (BNC)

Tally output : Voltage supply of 5 V DC (10 mA max.)

**Functions**

Signal format : NTSC color ("U" version) PAL color ("E" version)

Switching system : Vertical interval switching method

MIX : With fader lever

WIPE : 6 wipe patterns

Color background : Generates 8 colors. 1 of the 8 colors selectable

DSK : Generates 8 colors. 1 of the 8 insertion colors selectable

Chroma keying : RGB chroma key (blue-background), slice circuit and delay circuit provided

Synchronization : 2 modes, INT/EXT GENLOCK (with external VBS or BB) External genlock mode SC phase: COARSE (0°, 120° and 240° steps), FINE (±60° continuously variable)

**Performance**

Frequency response : 60 Hz to 5 MHz, ±0.3 dB (PGM output 5 to 8 MHz, $^{+0.3}_{-2}$ dB)

DG, DP : Less than 2 %, 2° (10 to 90 % APL)

S/N : More than 60 dB (p-p/rms)

Power supply : AC 100/120 V, 50/60 Hz ("U" version) AC 220/240 V, 50/60 Hz ("E" version) or DC12 V

Power consumption : AC 18 W/DC 1.2 A (12 V)

Operating temperature : 0 to 40°C (32 to 104°F)

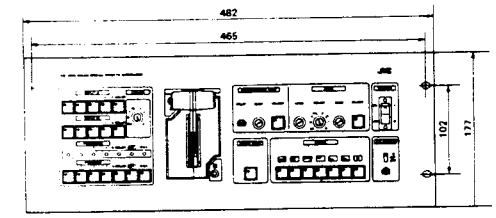
Weight : 4.2 kg (9.3 lbs)

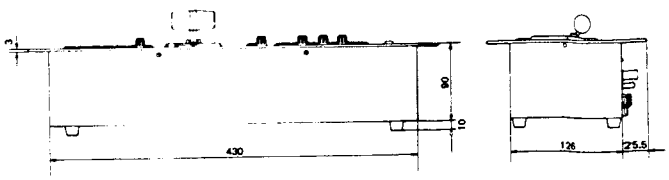
Dimensions : 482(W) x 177(H) x 100(D) mm (19" x 7" x 4")

**Accessory**

AC power cable : QMP9003-022 ("U" type) SCV0418-2M5 ("EG" type) SCV0419-2M5 ("EK" type) SCV0420-2M5 ("EA" type)

*Design and specifications are subject to change without notice.*




(unit: mm)

# CIRCUIT DESCRIPTION

## 1. SW BOARD/LO BOARD

### 1.1 BINARY CODE CONVERTER CIRCUIT (LO Board)

When inputs are selected using the INPUT A, INPUT B and PREVIEW bus line buttons (S1 to S17) on the control panel, the signals are converted into binary codes on the SW board and sent to the LO board as SW-DATA ①. The lines for these SW-DATA (A, B, C, GS) are common with the bus lines. Fig. 1 shows the binary code converter circuit. IC4 is an 8-input priority encoder, which is able to encode the signal with the highest priority among eight inputs (of which 7 are used in the KM-1200) into a 3-bit parallel signal. By outputting the input signals in the order of priority, operation errors due to double key strokes can be prevented.

The timing of key input signals on the three bus lines are shifted by the time-slot pulses ② for reading by IC4. This is necessary because the SW-DATA transmission lines are used in common as the bus lines. For instance, when one INPUT-A button and one INPUT-B button are pressed simultaneously, the SW-DATA signal can transmit these data by shifting the timing.

The time-slot pulses are generated on the LO board. Table 1 shows the SW-DATA signal statuses when the buttons are pressed. The same signals are generated when the same input is selected for different bus lines. The difference is that the same signals are transmitted with timing shifted for each bus line. These signals are generated when buttons are pressed and during the V blanking period.

| SW ON / DATA | 1 | 2 | 3 | 4 | 5/COLOR | EFF | DSK |
|---|---|---|---|---|---|---|---|
| A | H | L | H | L | H | L | H |
| B | H | H | L | L | H | H | L |
| C | H | H | H | H | L | L | L |
| GS | H | H | H | H | H | H | H |

**Table 1**

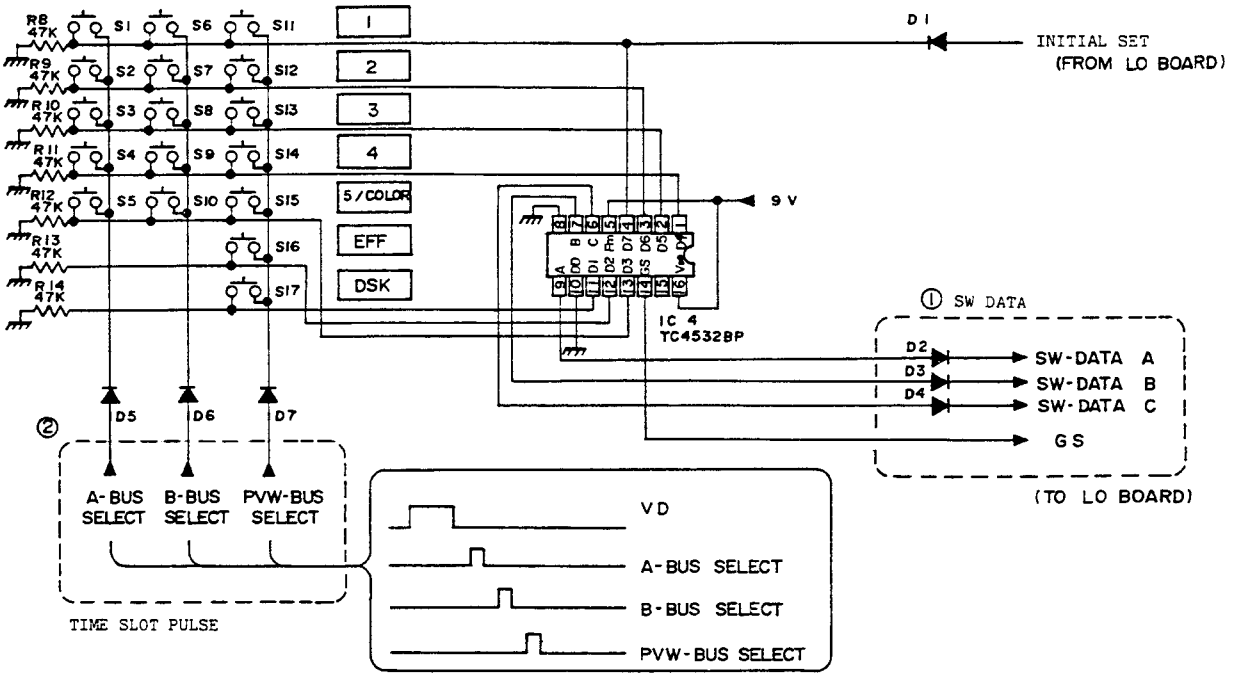



**Fig. 1** Binary code converter circuit

## 1.2 LATCH CIRCUIT (A-BUS LINE) (SW Board)

When the binary code signals (SW-DATA) are sent to the LO board, they should be latched because these signals are generated only when bus-line select buttons are pressed. Fig. 2 shows the latch circuit for the A bus.

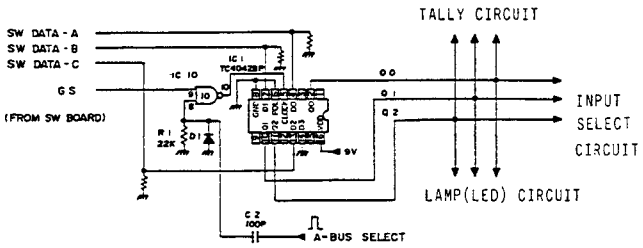



**Fig. 2** Latch circuit (A-bus line)

IC1 (TC4042BP) is a D-type flip-flop IC.
The SW-DATA signals of the A bus are latched at the instant when the clock signal turns from "L" to "H".
As the IC's clock signal coincides only with the A-bus time-slot pulse, IC1 reads only the A-bus SW-DATA signals. The B-bus and PVW line signals are respectively latched by IC2 and IC3 by a similar method.
The PGM bus signals are latched by IC4, by a slightly different method. Because that the PGM bus line signal is selected by taking the input signal selected for the PVW bus using the AUTO TAKE button. Therefore, IC4 uses the output of the preview bus line latch IC (IC3) as the input, and the AUTO-TAKE signal generated by pressing the AUTO TAKE button as the clock signal.
The latched signals are distributed into three branches, which are connected to the following circuits.

1. LED lighting circuitry (see 1.4) : SW board
2. Tally circuitry (see 1.5) : LO board
3. Crosspoint circuitry (see 3.1) : MA board

## 1.3 TIME-SLOT PULSE GENERATOR CIRCUIT (LO Board)

The time-slot pulse is important for the two following functions of the binary code converter circuit (1.1) and latch circuit (1.2).

1. Switching of the bus line signals in the V blanking period.
2. Common use as the SW-DATA signal transmission lines of the binary code converter circuit, by the A, B and PVW bus lines.

The time-slot pulses are generated by IC5 and IC12 on the LO board.
IC5 is a counter IC. It is reset by the fall of the VD pulse, reads HD as the clock, and generate time-slot pulses with the timing shown in Fig. 3. Because these pulses are to be generated only in the V blanking period, the rise of the output pulse from Q7 of IC5 is used to stop the counter during this period.

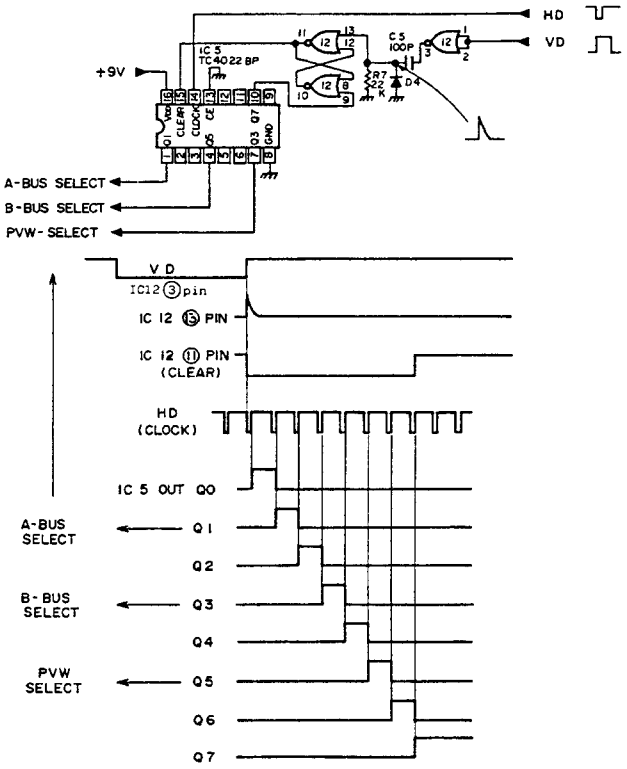



**Fig. 3** Time-slot pulse generator circuit

### 1.4 LED LIGHTING CIRCUIT (SW Board)

After being latched at the LO board, the SW-DATA signals return to the SW board. These signals are decoded by ICs 1, 2 and 3 on the SW board, in order to light LEDs by driving the LED drive IC2 (IC5, 6 and 7). Additional circuits are provided for the A bus line and B bus line to enhance the lighting of the LEDs in the select buttons during special effects modes (with "EFF" selected for the PGM bus). Fig. 4 shows the LED lighting circuit of the A bus line.

If, for example, "5/COLOR" is selected for the A bus line, the A-bus line SW-DATA signals (A, B, C) become (H, H, L) as shown in Table 2 and are input to decoder IC1. Q3 of IC1 then goes "H" as shown by Table 3, and the LED (S5) in the 5/COLOR button is lit via the inverter (—▷○—) of IC5.

The A-LIMIT signal is used to control additional circuits. It turns from "H" to "L" when the A-bus signal is used as the PGM output in the special-effects mode (EFF), and is supplied from the fader lever position detector circuit (see 1.6).

When the A-LIMIT signal goes "L", Q1 (switching transistor) turns ON to increase the current supplied to the LED. The lighting of the LED is thus enhanced.

### 1.5 TALLY CIRCUIT (LO Board)

When input signals selected for the bus lines are used for the PGM output, 5 V DC is output from the TALLY terminals on the rear panel to light the tally lamps of the cameras connected to the remote control units. Fig. 5 shows the tally circuit.

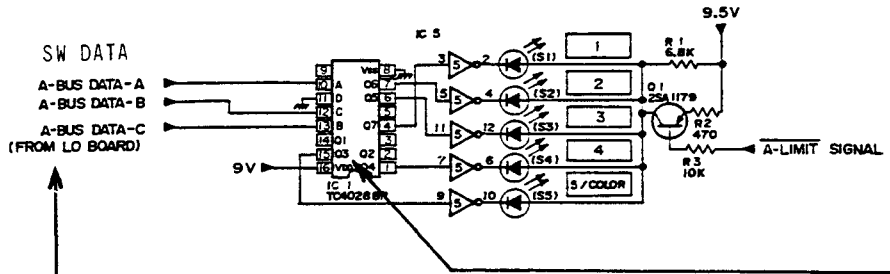



Table 1-2

| SW DATA \ ON | 1 | 2 | 3 | 4 | 5/COLOR | EFF | DSK |
|---|---|---|---|---|---|---|---|
| A | H | L | H | L | H | L | H |
| B | H | H | L | L | H | H | L |
| C | H | H | H | H | L | L | L |
| D | L | L | L | L | L | L | L |

Table 2

PREVIEW-BUS, PROGRAM-BUS ONLY

Table 1-3

| INPUT C | INPUT B | INPUT A | SELECTED OUTPUT "H" |
|---|---|---|---|
| L | H | L | Q 2 |
| L | H | H | Q 3 |
| H | L | L | Q 4 |
| H | L | H | Q 5 |
| H | H | L | Q 6 |
| H | H | H | Q 7 |

Table 3

**Fig. 4** LED lighting circuit (A bus line)

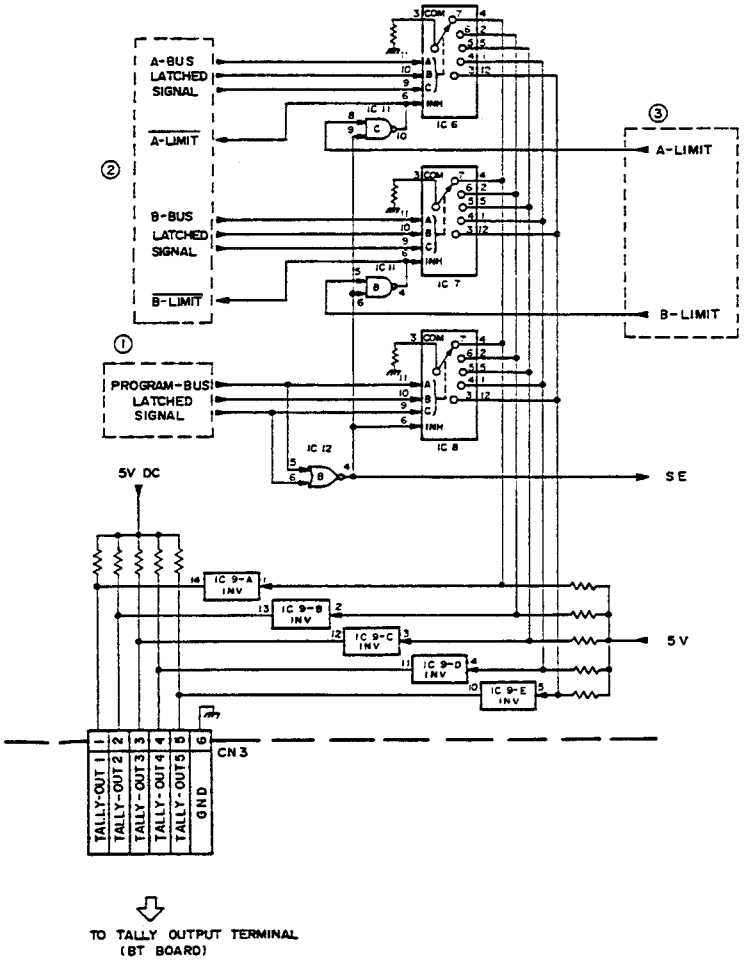
As described below, there are two methods for sending picture output signals to the PGM output. These methods use different tally control ICs.
(Tally control ICs : IC6, IC7, IC8)

1. Selecting one of "1" to "5/COLOR" of the PROGRAM but line buttons:
   Only IC8 operates to convert PROGRAM LATCHED signal ① into the tally control signal. Only one of tally outputs 1 to 5 is selected by this method.
2. Selecting the "EFF" PROGRAM bus line button and output the A-bus and B-bus outputs by controlling them using the fader-lever:
   IC6 and IC7 operate to convert A-BUS/B-BUS LATCHED signals ② into tally control signals. Normally, two tally outputs are selected. However, only one tally output is selected when the A-INPUT and B-INPUT buttons with the same number are pressed or when the fader lever is completely tilted towards "A" or "B".

IC6, IC7 and IC8 are multiplexers. The relationship between the input data (LATCHED signals ① and ② ) and output channels (tally outputs) is as shown in Table 5. The "ON" channels are connected to the COM terminal, but no channel goes ON when the INH terminal is "H". (Inhibit mode)

IC12 switches between IC8 and ICs 6 and 7. Its output goes "H" only when the "EFF" PROGRAM button is selected, inhibiting the operation of IC8. When one of the "1" to "5/COLOR" PROGRAM button is pressed, the IC12 output goes "L" and IC8 becomes operable.
The IC12 output is input to IC11 together with the fader-lever position detector circuit (see 1.6).
The IC11 output goes "L", making ICs 6 and 7 operable, when the following two conditions are met.

1. When IC12 output is "H" (when the "EFF" PROGRAM button is pressed).
2. When the fader-lever position detector circuit output is "H" (when the fader-lever is used to control the A-bus and B-bus signals).
   However, only IC6 operates when the fader-lever is completely tilted towards "A", and only IC7 operates when it is completely tilted towards "B".




LATCHED SIGNAL

| SW ON / DATA | 1 | 2 | 3 | 4 | 5/COLOR | EFF |
|---|---|---|---|---|---|---|
| A | H | L | H | L | H | L |
| B | H | H | L | L | H | H |
| C | H | H | H | H | L | L |

ONLY PROGRAM-BUS

**Table 4**

IC6/7/8 TRUTH TABLE

| CONTROL INPUTS | | | | "ON" |
|---|---|---|---|---|
| INHIBIT | C | B | A | CHANNEL |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |
| H | * | * | * | NONE |

* DON'T CARE

**Table 5**

**Fig. 5** Tally circuit

### 1.6 FADER-LEVER POSITION DETECTOR (LO Board)

This circuit detects the fader-lever position and generates the following two signals.

1. Fader-lever signal: Used by the WG board for the control of the wipe/mix circuit.
2. A-LIMIT and B-LIMIT signals: Input to the tally circuit (see 1.5) for the control of the tally IC. Also used for the control of the LEDs on the fader-lever section.

Fig. 6 shows the fader-lever position detector circuit.

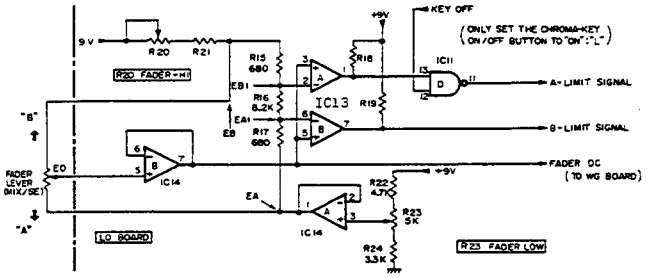



**Fig. 6** Fader-lever position detector circuit

Voltage $E_O$ depends on the position of the fader-lever. Upper limit $E_A$ of $E_O$ is set by R20 and lower limit $E_B$ by R23.

Fig. 7 shows the variation of IC13 output, A-LIMIT and B-LIMIT signals depending on the fader-lever position.

When the CHROMA KEY button is pressed "ON", the A-LIMIT signal goes "H" to operate the tally circuit, regardless of the fader-lever position (Fig. 7).

This operation is necessary because the chroma key effect is obtained by setting the fader-lever to "B" and both A-bus and B-bus signals are output at this time.

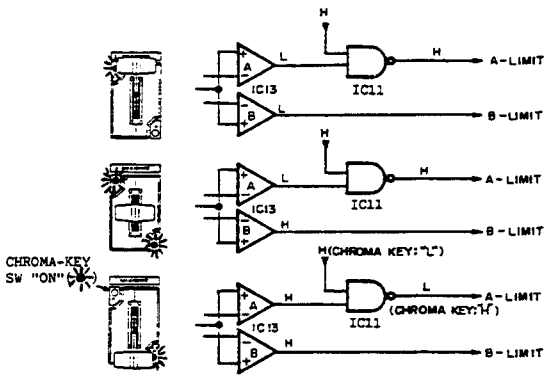



**Fig. 7** Variation of A/B-LIMIT signals

## 2. WG BOARD

The WG board has the following three functions.

1. SSG function
2. Wipe/mix control signal generation
3. Chroma key signal generation

2 and 3 are described in this section.

### 2.1 WIPE/MIX CONTROL SIGNAL GENERATION

The KM-1200 is provided with six wipe modes, and different video processing is performed depending on the mode used and the fader-lever position. Although the video processing is performed on the MA board, the details of processing is determined by the wipe control signal.

Fig. 8 shows the block diagram of the wipe/mix control signal generator circuit.

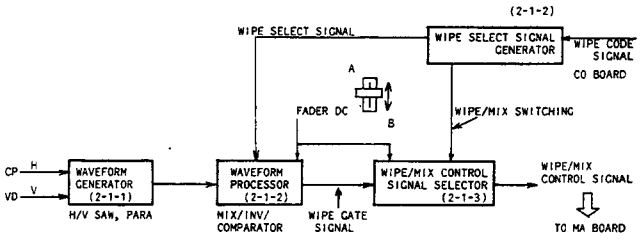



**Fig. 8** Block diagram of wipe/mix control signal generator

#### 2.1.1 Waveform generator circuit

This circuit generates the H and V sawtooth and parabolic waves required for wipe effects.

Fig. 9 shows the H waveform generator circuit.

The CP signal is integrated by the OP Amp in the primary stage to obtain the sawtooth wave. It is also integrated by the secondary-stage IC to obtain the parabolic wave.

The processing of the V period is the same as the H period except that the VD pulse is used as the source.

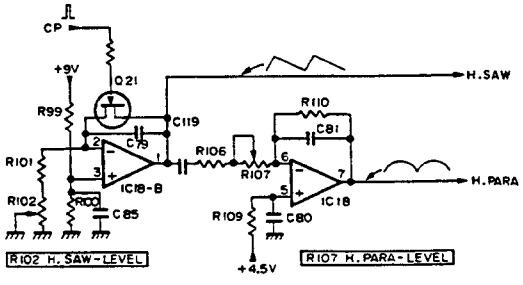



**Fig. 9** H-period waveform generator circuit

### 2.1.2 Waveform processor circuit

This circuit generates the wipe gate signals used for the wipe modes, from the H and V sawtooth and parabolic waves obtained by the waveform generator circuit (see 2.1.1).
The wipe gate signals are supplied to the wipe gate/mix control signal selector circuit and used by the wipe video processor circuit on the MA board.
Fig. 10 shows the waveform processor circuit.

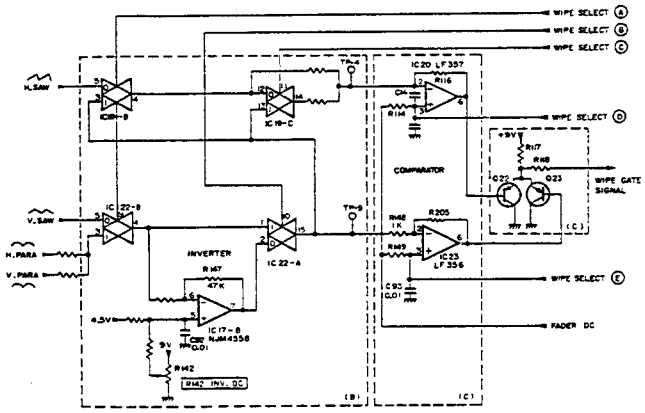


**Fig. 10** Waveform processor circuit

The wipe select signals (see 2.1.2 (A)) control the analog switches (ICs 19-B, 19-C, 22-B, 22-A) and comparators (ICs 20, 23) for the signal processing in each wipe mode.
Fig. 11 shows the process of signal processingl in each wipe mode.

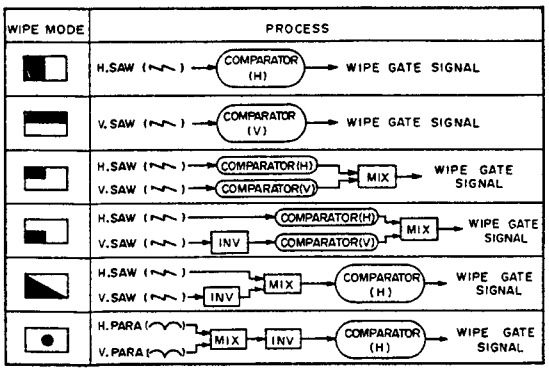



**Fig. 11** Signal processing in each wipe mode

(A) Wipe select signal generator:
This is the controller of the waveform processor circuit. Fig. 12 shows the wipe select signal generator circuit. When a wipe button is pressed, the CO board supplies the wipe code signals (see 4.2). These wipe code signals are decoded using IC24 to obtain wipe select signals.

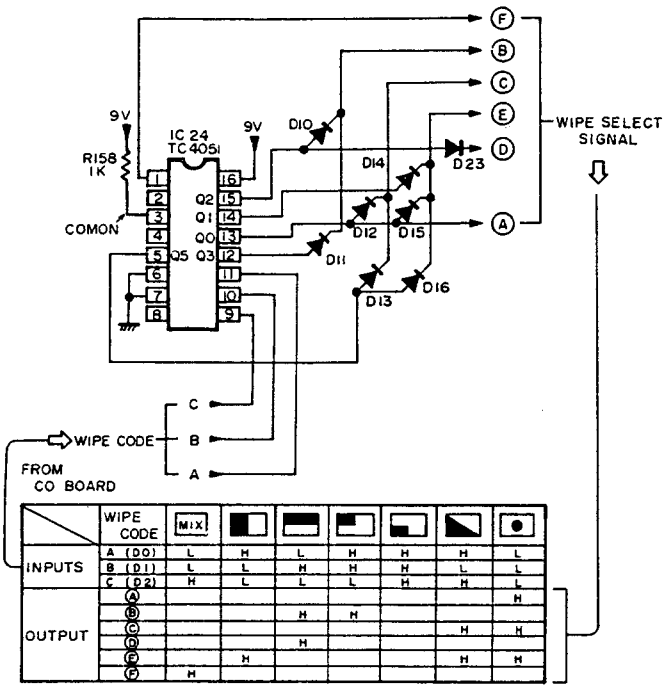
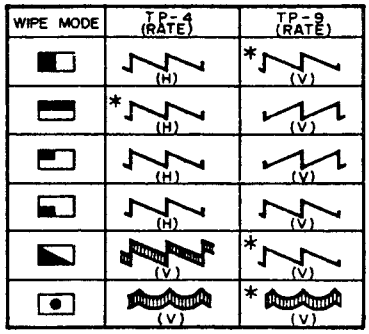



**Fig. 12** Wipe select signal generator circuit

Wipe select signals Ⓐ Ⓑ Ⓒ control the analog switches (ICs 19-B, 19-C, 22-B, 22-A), and signals Ⓓ Ⓔ control the comparators (ICs 20, 23). (See Fig. 10.) Signal Ⓕ is used to control the wipe/mix control signal selector circuit. (See 2.1.3.)

(B) SAW/PARA selector circuit:
In this circuit, analog switches are switched by wipe select signals Ⓐ Ⓑ Ⓒ to select the V and H sawtooth and parabolic waves. (See Fig. 10.)
The signals selected by this circuit for each wipe mode can be checked at TP4 and TP9.
Fig. 13 shows the waveforms observed at TP4 and TP9.




**Note:** Waveforms marked * are not used actually.

**Fig. 13** Waveforms at TP4 and TP9

(C) Comparator circuit and H/V mixer circuit:
The SAW/PARA output signal (see 2.1.1(B)) and fader-lever signal (see 1.6) are compared to determine the wipe gate signal output. (See Fig. 10.)
The fader-lever signal voltage depends on the fader-lever position. The wipe gate signal goes "L" when the SAW/PARA selector circuit output voltage is higher than the fader-lever signal voltage, and goes "H" when it is lower. When wipe select signal Ⓓ or Ⓔ goes "H", IC20 or IC23 respectively is inhibited and the output is not supplied. The outputs from the comparators are mixed by Q22 and Q23 to become the wipe gate signal.

### 2.1.3 Wipe/mix control signal selector circuit

When a wipe mode button among the MODE buttons on the control panel is pressed, wipe select signal Ⓕ goes "L" and the wipe gate signal is used as the wipe control signal. When the MIX button is pressed, wipe select signal Ⓕ goes "H" and the DC voltage obtained by tilting the fader-lever (fader-lever signal) is used as the mix control signal.

## 2.2 CHROMA-KEY SIGNAL GENERATOR CIRCUIT

With the chroma-keying effect, the key pulse generated by utilizing the hue differences of the camera's R/G/B signals is mixed with the wipe/mix control signal, for the insertion of a video signal by replacing the part corresponding to the key pulse n the key camera's video signal.

### 2.2.1 Reference hue signal generator circuit

This circuit generates the reference hue signal from the R/G/B signals supplied from the key camera, in order to obtain the key pulse.
The inverted B CH signal is output at the collector of Q30. On the other hand, the R/G CH signals are mixed through R161 and R162, amplified by Q29, and output at the collector of Q30 with positive phase. As a result, an R + G – B signal output can be obtained.
R168 (W. BAL) is a VR for adjustment so that 1/2(R + G) – B = 0 when the input signal is all-white or all-black.

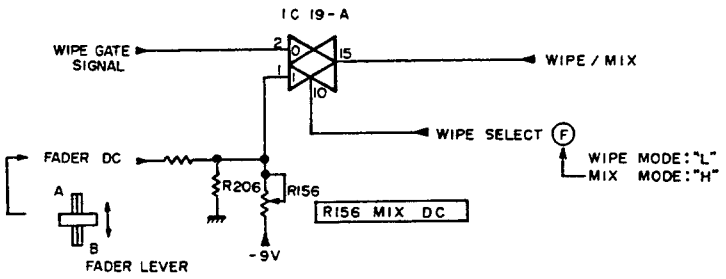
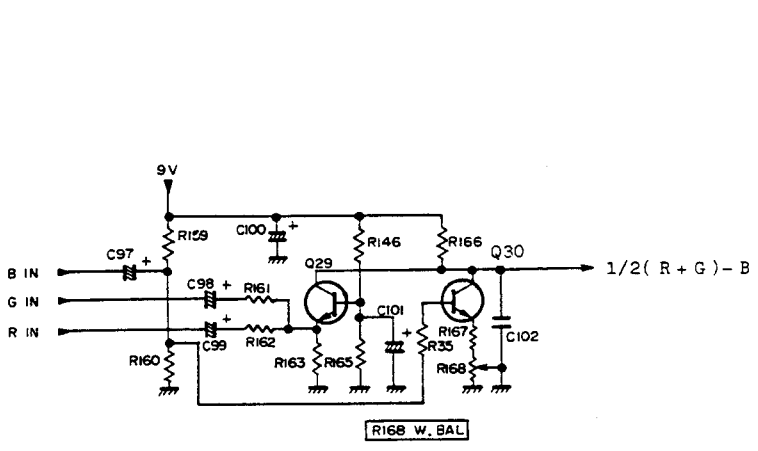
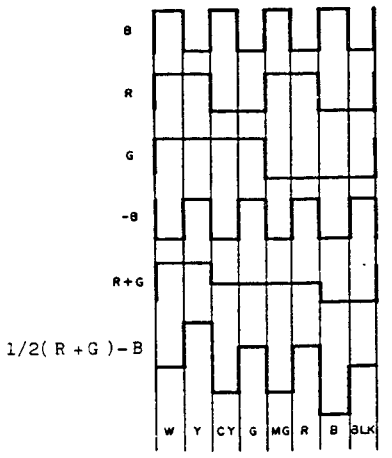



**Fig. 14** Wipe/mix control signal selector circuit




Example of color bars

**Fig. 15** Reference hue signal generator circuit

### 2.2.2 Key delay circuit

As there is a phase difference between the key camera's R/G/B signals and the keying VBS (composite video signal), their timings are aligned by delaying the reference hue signal. The amount of delay is approx. 0.65 μs is also possible using the DELAY potentiometer (= R29, KEY DELAY, on the CO board) on the control panel.

### 2.2.3 Clamp circuit and comparator

After being output from the key delay circuit, the reference hue signal passes through Q31 (amp) and Q32 (buffer), and is clamped at Q38. The clamping pulse is the BF (burst flag) pulse and clamping potential is 4.5 V DC.

The clamped signal is input to the ⊖ input of IC25 and is compared with the ⊕ input from R181 (KEY SLICE), so that the part above the ⊕ input is shaped into a positive pulse and the part below it into a negative pulse. The shaped signal is mixed with the wipe/mix control signal for use in actual waveform processing on the MA board.

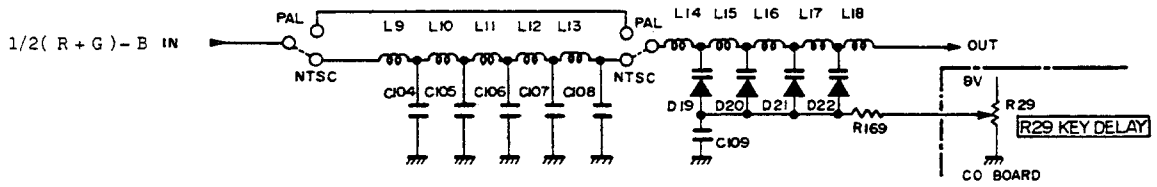



**Fig. 16** Key delay circuit

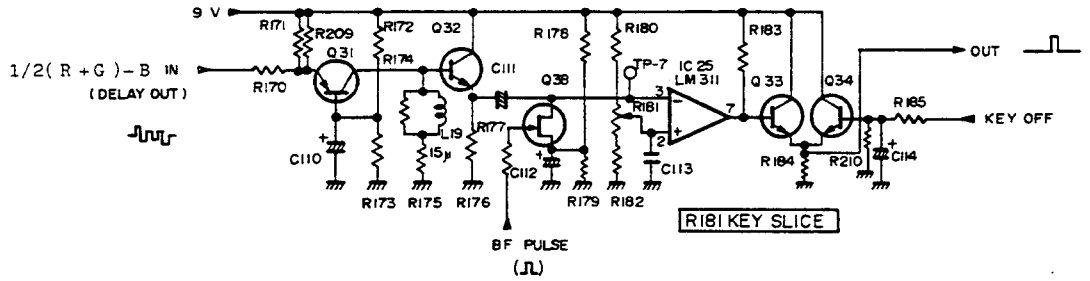



**Fig. 17** Clamp circuit and comparator

## 3. MA BOARD

The MA board processes the video signal using the wipe gate signal generated at the WG board. The operations of the processor circuits are as follows.

### 3.1 CROSSPOINT CIRCUIT

This circuit selects the input video signals necessary for special effects. Inputs signals of channels 1 to 5 can be switched to the A, B, PGM and PVW bus lines.

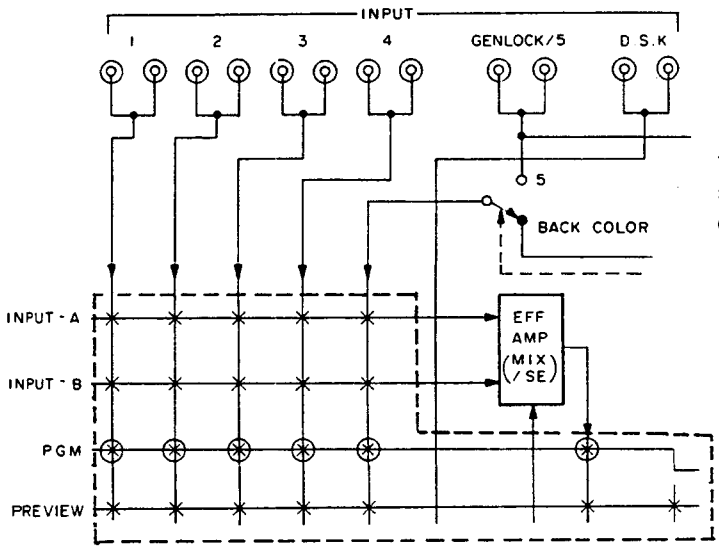



**Fig. 18** Crosspoint circuit

Fig. 19 shows the input select circuit for the A bus line.

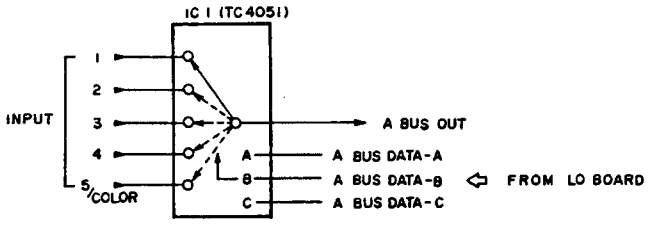



**Fig. 19** A bus line input select circuit

### 3.2 VIDEO SIGNAL PROCESSOR CIRCUIT

This circuit processes the input video signals selected by the crosspoint circuit (see 3.1) for generating a number of special effects. Fig. 20 shows the block diagram of this circuit.

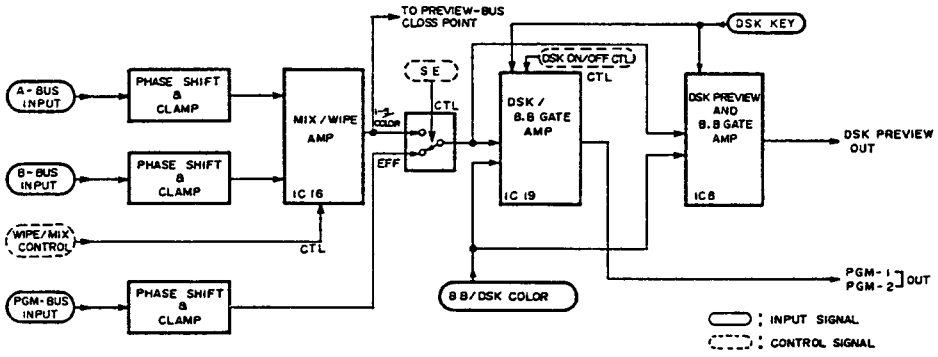



**Fig. 20** Block diagram of video signal processor circuit

### 3.2.1 Phase-shift and clamp circuits

Video signals selected for the bus lines pass through the phase shift and clamp circuits before being input to the mixing amp. Fig. 21 shows the circuit of the B bus line.

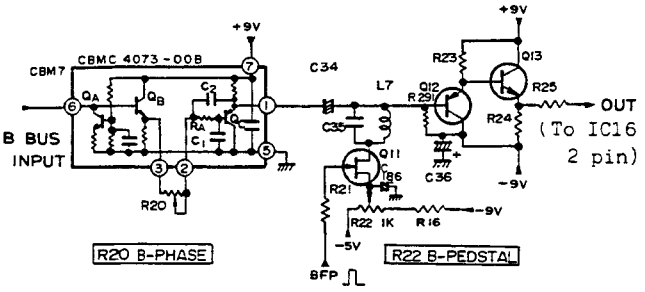



**Fig. 21** Phase-shift and clamp circuits

CBM7 is a phase shifter including a low-pass filter. $Q_A$ and $Q_B$ form the buffer for the input select circuit, and C1, C2, $R_A$, R20 and $Q_C$ form the LPF.

The SC width which is 279 ns with NTSC and 226 ns with PAL, may contain phase error due to the propagation delay of transistors and the stray capacitance of the PCB.

As it is necessary to match the chroma phases when mixing the A and B bus lines, the B bus phase is adjusted by R20 to coincide with that of the A bus.

The CBM7 output signal is clamped by BFP at Q11, supplied through buffers Q12 and Q13, and input to the wipe/mix amp IC. Clamping is possible without affecting the input signal burst thanks to the parallel-resonance tank circuit of L7 and C35 which increases the impedance. R22 is used to match the B bus pedestal level with that of the A bus.

### 3.2.2 Wipe/mix amp circuit

The wipe/mix amp circuit processes the waveforms of the A-bus and B-bus input signals to obtain the wipe/mix effect. Fig. 22 shows the wipe/mix amp circuit.

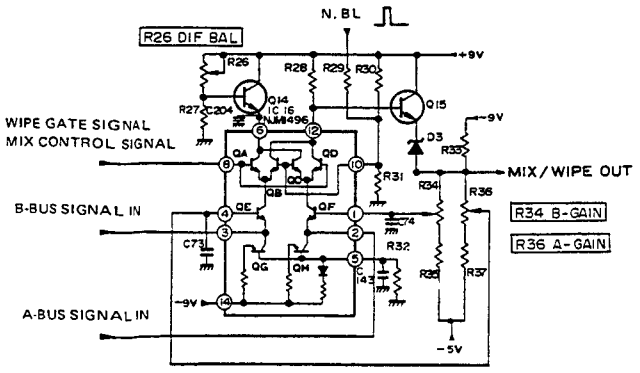



**Fig. 22** Wipe/mix amp circuit

IC16 is a balanced modulator IC (NJM1496). It has double-balanced differential amplifier construction in which $Q_A$ and $Q_C$, $Q_B$ and $Q_D$ are respectively connected to the common loads of Q14 and R28.

$Q_G$ and $Q_H$ are regulated current supplies. The currents flowing to $Q_E$ and $Q_F$ vary depending on the input A bus and B bus signals.

To control the output gain of IC16, the bases of $Q_E$ and $Q_F$ are supplied with the feedback voltage determined by R34 (B-GAIN) and R35 (A-GAIN).

The wipe/mix control signal generated on the WG board (see 2.1) is applied to the bases of $Q_A$ and $Q_B$ via IC16 pin ⑧ . The bases of $Q_B$ and $Q_C$ are applied with the narrow blanking (N. BL) pulse which has a relatively small blanking width.

Fig. 23 shows the IC16 output waveforms when the A-bus input is a white signal, the B-bus input is a black signal and the "■□" wipe button has been pressed.

When the timing of N. BL is "H", $Q_B$ and $Q_C$ are saturated (ON) and the A bus signal is output from pin ⑫ during this period.

When N. BL goes "L", $Q_B$ and $Q_C$ go ON or OFF depending on the DC level of the wipe/mix control signal (or the wipe gate signal during wipe gating). Namely, when the wipe gate signal is "H", $Q_A$ and $Q_D$ turn ON and the B bus signal is output. When the wipe gate signal is "L", $Q_C$ and $Q_B$ turn ON and the A bus signal is output. The waveforms shown in Fig. 23 are obtained in this way.

In the mix mode, the mix control signal (DC) is applied to IC16 in place of the wipe gate signal. This DC voltage is set within the range that can vary $Q_A$, $Q_B$, $Q_C$ and $Q_D$ between the saturation and cutoff levels by moving the fader-lever. This makes it possible to mix the A-bus and B-bus signals.

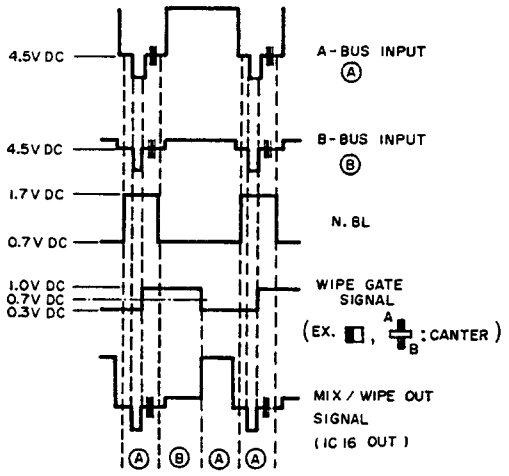



**Fig. 23** IC16 input/output signal waveforms

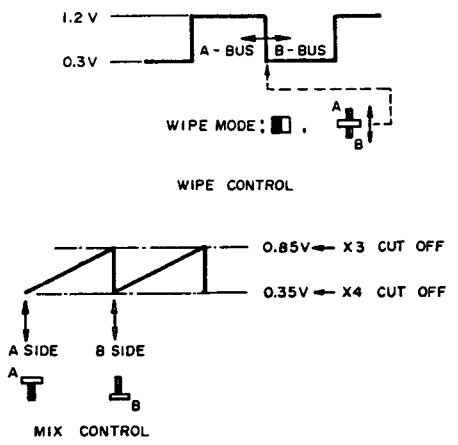



**Fig. 24** Variations of wipe/mix control signals

### 3.2.3 DSK/BB gate amp circuit

Although the circuit construction of the DSK/BB gate amp is similar to that of the wipe/mix amp described in 3.2.2, its functions are different.

After keying to the main line signal using the keying signal input at the DSK input connector, the color signal generated by the DSK color generator (see 3.3) is added to it. Fig. 25 shows the circuit diagram and input/output waveforms.

When the DSK ON/OFF button on the control panel is "OFF", only a DC voltage is applied as DSK key signal Ⓓ. At this time, keying not performed while reinsertion of the burst and sync signals is always performed.

### 3.2.4 Preview/BB gate amp (IC18)

This circuit supplies the DSK preview signal, which is the main line signal keyed by the DSK input signal, at the DSK PREVIEW connector on the rear panel, regardless of the setting of the DSK ON/OFF button. Its circuit configuration is similar to the DSK/BB gate amp above. (See 3.2.3.)

## 3.3 DSK COLOR GENERATOR CIRCUIT

With the DSK effect, keying to the main line signal is performed using the DSK input signal, and color signal is inserted into the keyed part. The DSK color generator circuit generates the color signal to be inserted into the keyed part.

### 3.3.1 DSK color pulse

When a color is selected on the DSK color control on the control panel, the WG board supplies the DSK color select signals (A, B, C) as shown in Fig. 26. These signals are NANDed with the DSK key signal to generate the DSK color pulse. The DSK key signal is obtained from the signal input to the DSK INPUT connector on the rear panel.

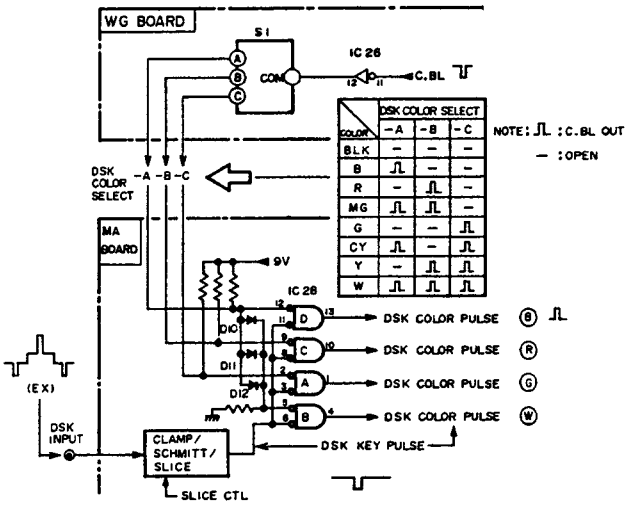



**Fig. 26** DSK color pulse generator circuit

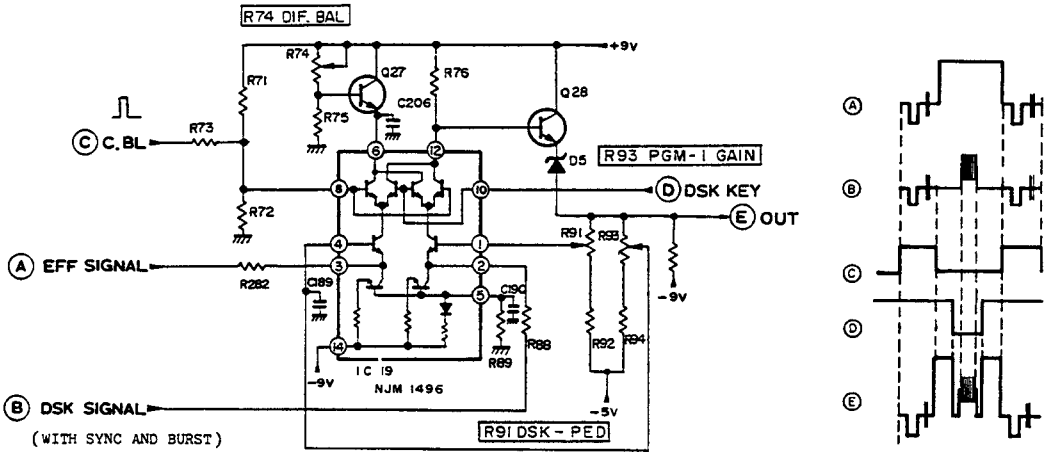



**Fig. 25** DSK/BB gate amp circuit and its waveforms

DSK color pulse Ⓑ outputs the inverted DSK key pulse when the selected color is B/Mg/Cy/W.
Similarly, Ⓡ outputs the inverted signal for R/Mg/Y/W, and Ⓖ outputs it for G/Cy/Y/W. In other cases, the output is always "L".

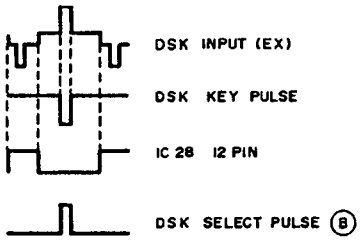



**Fig. 27** When B is selected

### 3.3.2 Y signal/color signal generattion

DSK color pulses Ⓑ Ⓖ Ⓡ are mixed through R155, R156 and R157 (see Fig. 28) to become the Y signal. The Y signal is amplified by Q44 then distributed into two paths.

One path is to the emitter of Q46, where it is mixed with DSK color pulse Ⓦ , amplified by Q63, then supplied to the LC type delay circuit for phase matching with the color difference signals described later. The output is amplified by Q64 and becomes the Y signal.
The other path is from Q47 and is used to generate the color difference signals (B-Y, R-Y).
Color difference signal B-Y is inverted by Q48 to become the Y-B signal. After being filtered at 0.5 MHz by C89, C90, R172 and R286, it is mixed with the BFP and input to the encoder for generating the burst signal.
The R-Y signal is also generated similarly and input to the encoder IC.

### 3.3.3 Encoder

IC29 is the encoder IC which modulates B-Y and R-Y using SC and mixes them with the Y signal. By this operation, the output at the emitter of Q54 has the DSK color signal added to the keyed part.

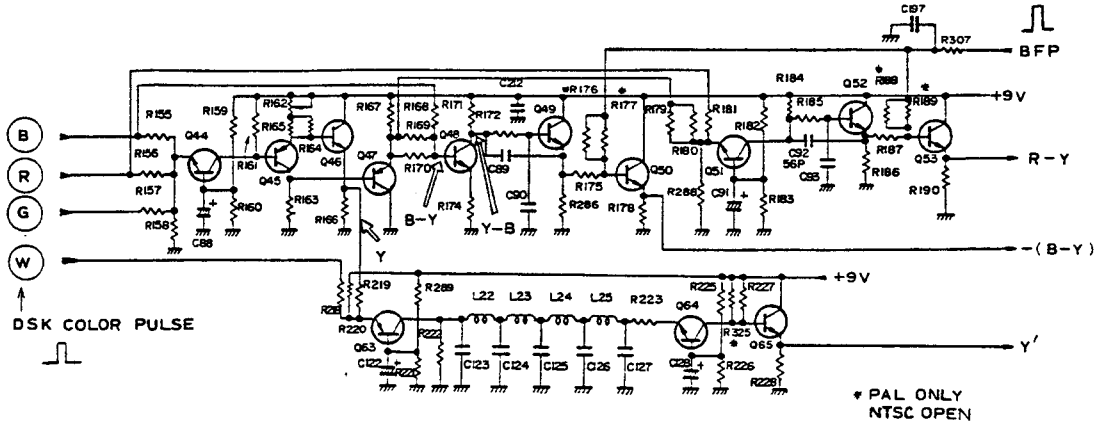



**Fig. 28** Y signal/color difference signal generator

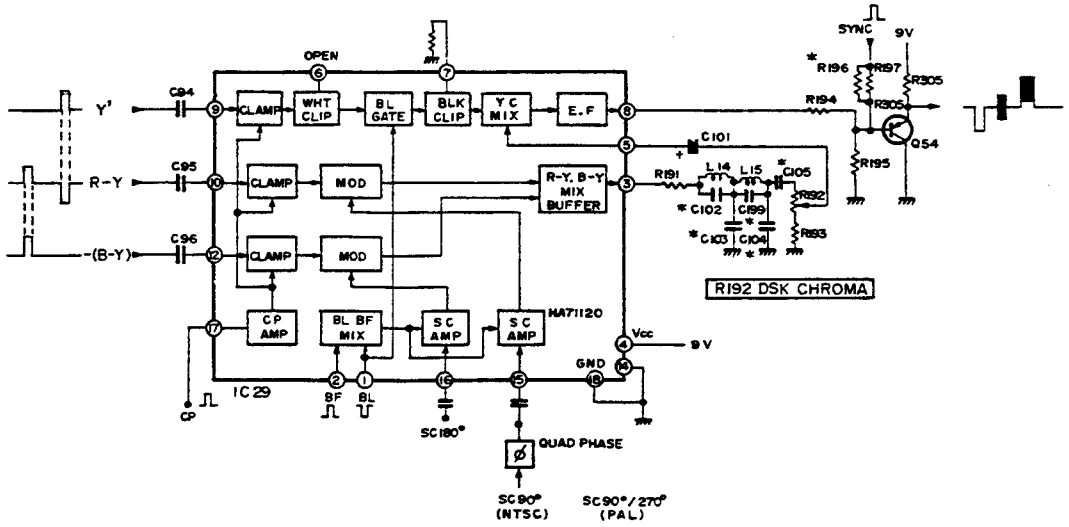



**Fig. 29** Encoder IC

## 4. CO BOARD

This CO board consists of the following circuits.

1. Genlock signal sync separator circuitry
   (1) Sync separator
   (2) H pulse generator
   (3) Genlock signal presence detector
   (4) Burst gate pulse generator
2. Wipe mode selector circuitry
   (1) Binary code converter
   (2) Selected signal latch
   (3) LED indicator circuit
3. Switch signal generator circuit
   (1) Chroma keying ON/OFF signal
   (2) DSK ON/OFF signal
   (3) AUTO-TAKE signal
   (4) Initial setting pulse
4. SC phase shifter circuit

### 4.1 GENLOCK SIGNAL SYNC SEPARATOR CIRCUITRY

#### 4.1.1 Sync separator

Fig. 30 shows the sync separator circuit.

The genlock signal (VBS or BB) is input to the base of Q4, and the inverted signal is output from the collector. This signal is filtered by the LPF composed of R33, C26 and C11, sent through Q5 (emitter-follower) and Q7 (amp), and output from the collector of Q7 as the separated sync signal. This signal is then distributed into two paths. One is used for the detection of the presence of the genlock signal (see 4.1.3). The other, after being differentiated by Rx and C14, is converted to a clamping pulse by Q8 and goes to the base of Q9. As the emitter of Q9 is grounded, the genlock signal at the collector of Q9 is clamped at the GND potential.

The clamped genlock signal is sent to Q10 (buffer), held, and integrated by R43 and the WG board C118, to become DC. It is then supplied through Q11, divided into 4 : 6 by R45 and R46, and input to the base of Q12. On the other hand, the base of Q13 is supplied with the genlock signal from the base of Q6, the pedestal of which is clamped at the GND level. As Q12 and Q13 form a differential amp, the part of the input signal which is higher than the voltage at the base of Q12 is output from the collector of Q13 as the separated sync signal.

#### 4.1.2 H sync pulse generator

IC8-A is a one-shot multivibrator, the trigger input of which is the sync signal separated from the genlock signal. As the V sync signal includes serrated or equalizing pulses, they are eliminated by IC8-A, when A-trigger input is "H", B-trigger input becomes inhibit mode. By supplying output Q to input A, so that re-triggering due to the equalizing pulse is eliminated and it can be output from Q as an H sync pulse. The width of T is determined by C20, R49 and R50. (60 $\mu$sec > T > 32 $\mu$sec)

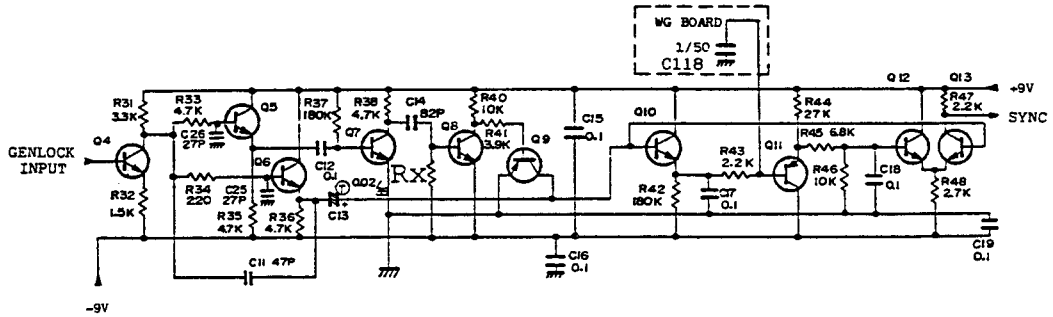



**Fig. 30** Sync separator

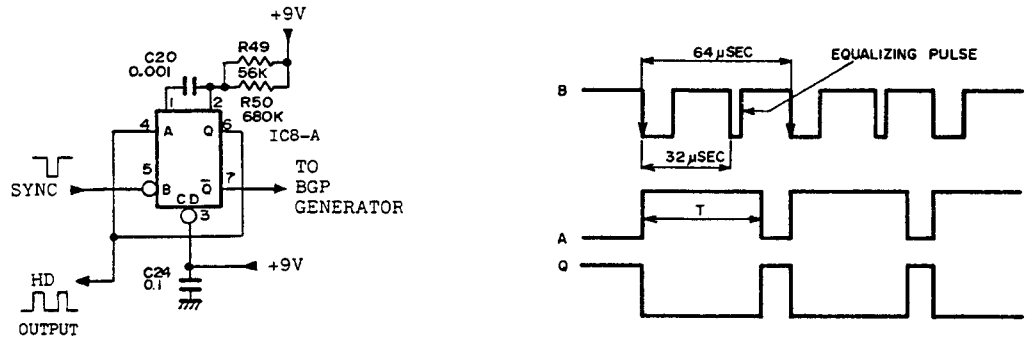



**Fig. 31** H sync pulse generator

### 4.1.3 Genlock signal presence detector

The separated sync signal from Genlock signal is input to trigger input B of IC8-B. As the time constant of C21 and R151 has been set sufficiently longer than the H. SYNC period, re-triggering is repeated as long as the input signal is present, and the output Q is maintained at "H". When there is no input, Q turns "L" so it can be judged whether the sync is internal or external.

H. SYNC is shaped by C27, D13, D12, R61 and C28 to obtain a positive voltage, which maintains IC8 active to prevent malfunctions due to noise, etc. (The CD terminal is reset by "L".)

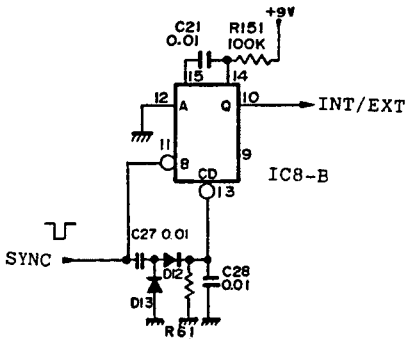



**Fig. 32** Genlock signal presence detector

### 4.1.4 Burst gate pulse generator

Similarly to 4.1.2 and 4.1.3, the burst gate pulse is generated using one-shot multivibrators IC9-A and IC9-B. IC9-A determines the burst gate pulse start position by triggering of the fall of the sync signal separated from the genlock signal. IC9-B determines the burst gate pulse width by triggering at the fall of the IC9-A output. The two output pulse widths are determined by C22 and R52, and C23 and R53.

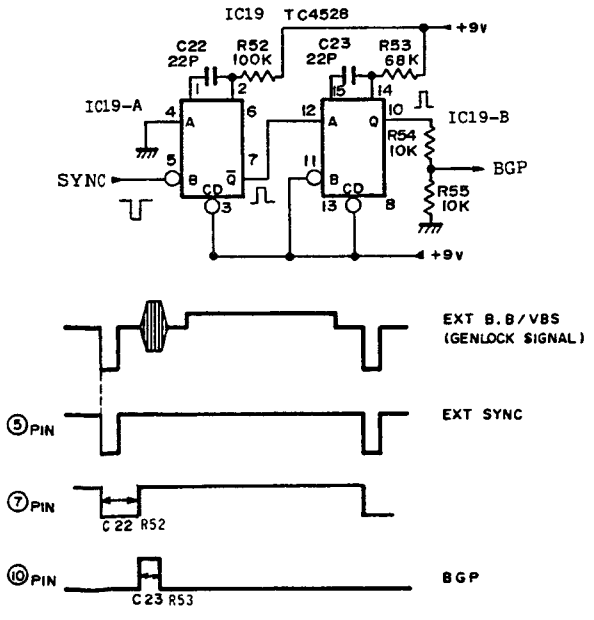



**Fig. 33** Burst gate pulse generator

## 4.2 WIPE MODE SELECTOR CIRCUITRY

### 4.2.1 Binary code converter

IC1 is an 8-bit priority encoder, which converts switch signals S1 to S7 into binary codes when a wipe mode is selected by a MODE select button on the control panel. The inputs (D0 to D7) to IC1 are usually "L", and one of them goes "H" only when one of S1 to S7 is pressed. The outputs (Q0 to Q2) are as shown in Table 6.

| | INPUT | | | | | | | | OUTPUT | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_{IN}$ | | – | | MIX | | | | | GS | Q2 | Q1 | Q0 | $E_{OUT}$ |
| L | * | * | * | * | * | * | * | * | L | L | L | L | L |
| H | L | L | L | L | L | L | L | L | L | L | L | L | H |
| H | H | * | * | * | * | * | * | * | H | H | H | H | L |
| H | L | H | * | * | * | * | * | * | H | H | H | L | L |
| H | L | L | H | * | * | * | * | * | H | H | L | H | L |
| H | L | L | L | H | * | * | * | * | H | H | L | L | L |
| H | L | L | L | L | H | * | * | * | H | L | H | H | L |
| H | L | L | L | L | L | H | * | * | H | L | H | L | L |
| H | L | L | L | L | L | L | H | * | H | L | L | H | L |
| H | L | L | L | L | L | L | L | H | H | L | L | L | L |

* DON'T CARE

**Table 6**

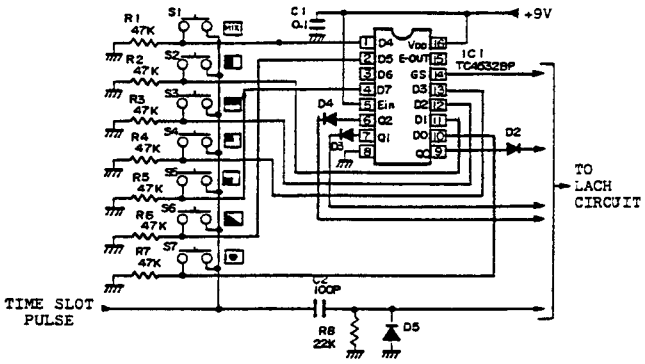



**Fig. 34** Binary code converter

### 4.2.2 Selected signal latch

It is necessary to latch the IC1 outputs because they are generated only when a MODE button is pressed. IC2 performs latching, using the IC5 output as the clock input. Pin ⑤ of IC5 is supplied with the GS output from IC1, which goes "H" when one of D0 to D8 is input. Pin ⑥ is supplied with the time-slot pulse (see 1.3.5) differentiated by C2, R8 and D5, which goes "H" 6H after the end of VD pulse. As a result, when one of wipe mode select buttons (S1 to S7) is pressed, the signal is latched in the first V. BL period after the button is pressed.

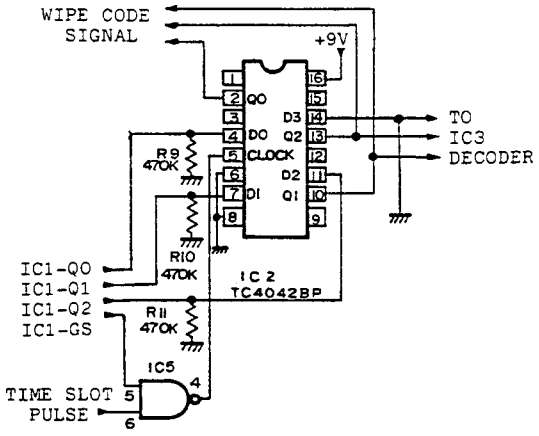



**Fig. 35** Latch circuit

### 4.2.3 Indicator circuit

The wipe code signal is decoded by IC3 after latched and supplied to the LED drivers IC4 and IC5 for lighting of an LED. For example, when the "■□" wipe mode button is pressed on the control panel, the DATA signals (A, B, C) become (H, L, L) which are input to decoder IC3. Then Q1 output turns "H" as shown in the Table in Fig. 36, so that the LED (S2) in the "■□" button is lit via the inverter of IC4.

The SE signal, which is supplied from the WG board, goes "L" when the "EFF" PGM output is selected. With this signal input, Q1 turns ON, the series resistance between the LED and power supply drops and the LED current increases. As a result, the illumination of the LED is enhanced when the "EFF" PGM output is selected.

## 4.3 SWITCH SIGNAL GENERATOR CIRCUITRY

### 4.3.1 Chroma keying ON/OFF signal generator

In Fig. 37, S8 is the CHROMA-KEY ON/OFF switch and IC6 is a NAND Schmitt circuit. When S8 is pressed, the input at pin ① of IC6 goes "L", pin ③ outputs waveform-shaped "H", which is input to pin ③ of IC7. D flip-flop IC7 operates as an ordinary flip-flop because output $\overline{Q}$ is returned to input D. When pin ③ of IC7 goes "H", $\overline{Q}$ goes "L" at that timing, and it is output to the WG board via at the same time lighting the LED in S8. When the CHROMA-KEY ON/OFF switch is pressed again, IC7 output $\overline{Q}$ turns "H" and the LED (S8) goes off.

### 4.3.2 DSK ON/OFF signal generator

The operation is the same as that of the chroma keying ON/OFF signal generator (see 4.3.1).

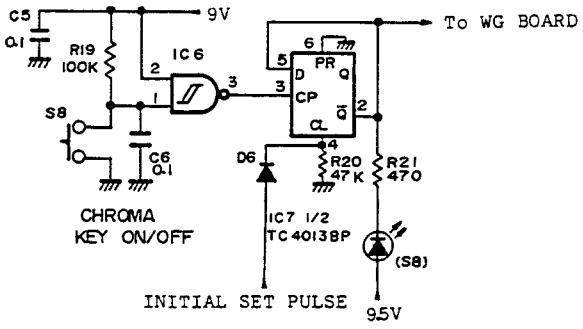
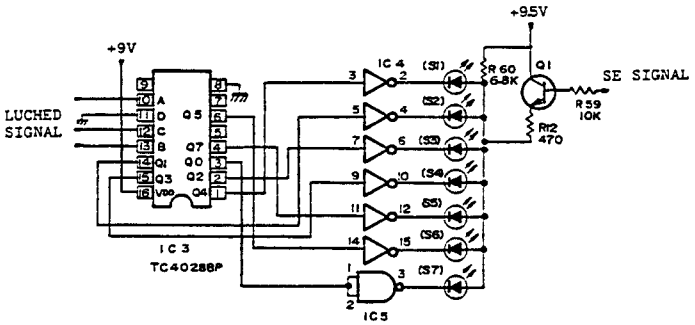



**Fig. 37** Chroma keying ON/OFF signal generator




| INPUTS | | | | SELECTED OUTPUT "H" |
|---|---|---|---|---|
| D | C | B | A | |
| L | L | L | L | Q0 |
| L | L | L | H | Q1 |
| L | L | H | L | Q2 |
| L | L | H | H | Q3 |
| L | H | L | L | Q4 |
| L | H | L | H | Q5 |
| L | H | H | H | Q7 |

IC3 TRUTH TABLE

**Fig. 36** Indicator circuit

### 4.3.3 AUTO TAKE signal generator

When the AUTO TAKE button (S10) on the control panel is pressed, the IC6 input goes "L" and the output goes "H". This AUTO TAKE signal is supplied to the LO board via the WG board. It is also supplied to inverter IC5 to light the LED in the AUTO TAKE button. (The LED goes off when the button is released.)

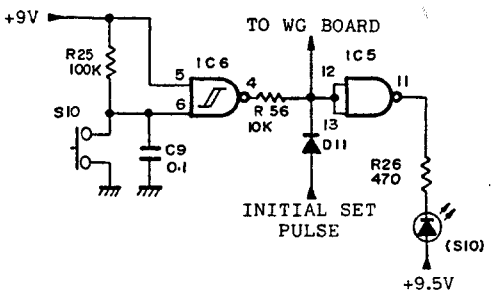



Fig. 38 AUTO TAKE signal generator

### 4.3.4 Initialization pulse generator

By the operation of the integration circuit of R27 and C10, the waveform input to IC6 immediately after turning power on is as shown in Fig. 39. It is "H" until the level exceeds the value determined by D8 and "L" when it exceeds this value, providing a pulse as a result. This pulse is used as the initialization pulse by the CO board and LO board.

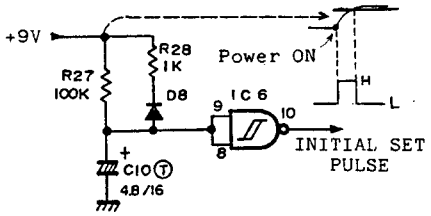



Fig. 39 Initialization pulse generator

### 4.3.5 SC phase shifter

Q2, C4 and R17 form an active LPF. The phase of the SC input from the WG board is adjusted (delayed) by R17, and the signal is output from the emitter of Q3.

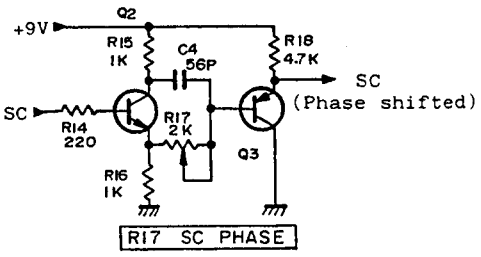



Fig. 40 Phase shifter

# SECTION 1
# DISASSEMBLY

## 1.1 BEFORE DISASSEMBLING

Before disassembling, study this section carefully.

### 1.1.1 Replacement of main fuses

Open the control panel referring to Sec. 1.2.1 open of control panel.

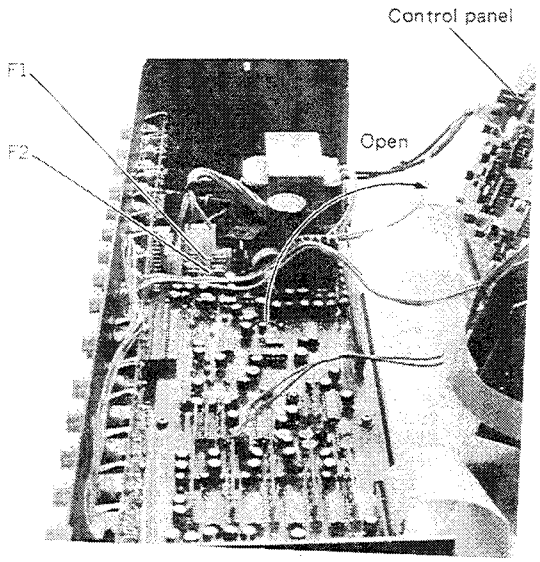



Fig. 1-1

| | Line Voltage | Fuse | |
|---|---|---|---|
| Secondary side | +10 V | F1 (1.6 A) | USA/CAN/120V: QMF51J1-1R6<br>220/240 V: QMF51A2-1R6 |
| | +12 V | F2 (1.6 A) | USA/CAN/120 V: QMF51J1-1R6<br>220/240 V: QMF51A2-1R6 |

Table 1-1

### 1.1.2 Removal of knobs

1. Pull up and remove the knobs.

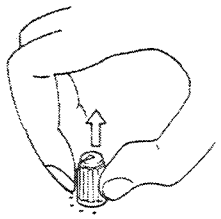


Fig. 1-2

### 1.1.3 Replacement of key top

Pull off the key top with a finger tip or a screwdriver by inserting its tip into the key slot.

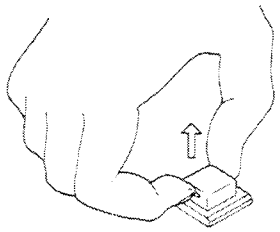


Fig. 1-3

### 1.1.4 Card fit cable connection

Note for conductors side on both of card cable and connector to mate.

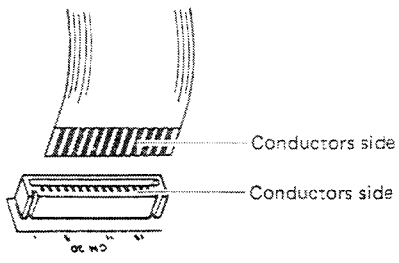



Fig. 1-4

## 1.2 DISASSEMBLY

### 1.2.1 Open of the control panel

Loosen six screw (1) of the side panel and open the control panel in the direction in Fig. 1-6.

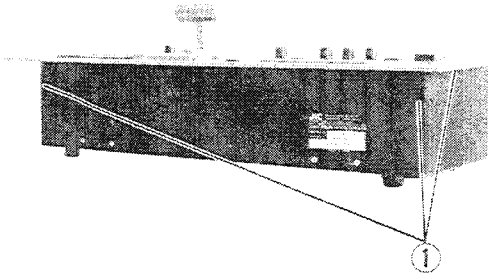



Fig. 1-5

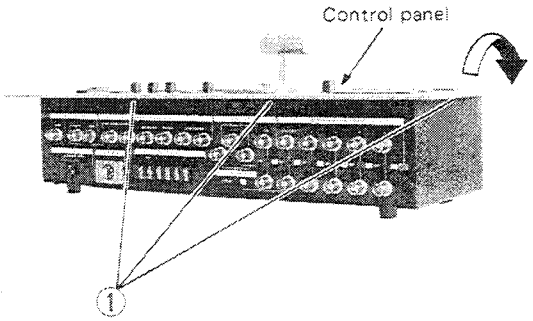



Fig. 1-6

### 1.2.2 Removal of WG/LO boards

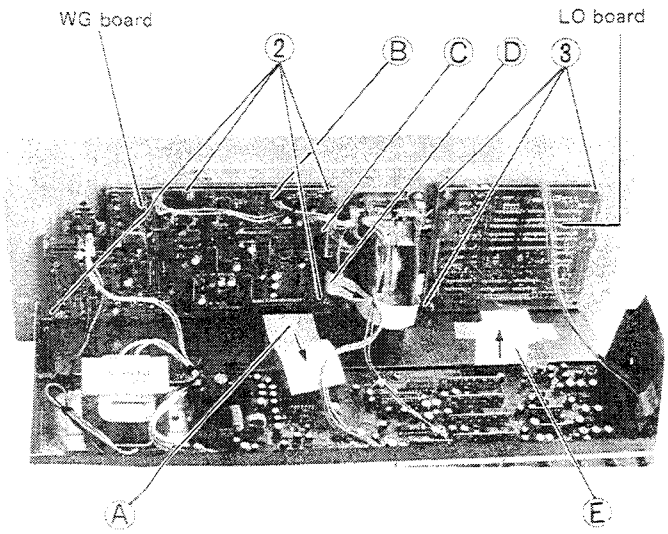



Fig. 1-7

- Removal of WG board

1. Remove the card fit cables (A), (D), from the connectors.
2. Remove the connectors (B), (C).
3. Remove the four screw (2) and remove the WG board.

- Removal of LO board

1. Remove the card fit cables (D), (E).
2. Remove the three screws (3) and remove the LO board.

### 1.2.3 Removal of CO/SW boards

- Remove the knobs on the control panel according to 1.1.2.

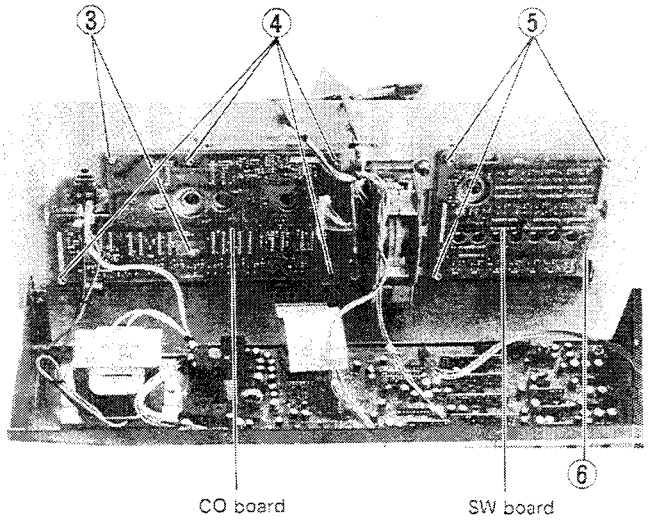



Fig. 1-8

- Removal of CO board

1. Remove WG board according to 1.2.2.
2. Remove a screw (3) in the Fig. 1-8.
3. Remove the four stud screws (4) and remove the CO board.

- Removal of SW board

1. Remove LO board according to 1.2.2.
2. Remove screw (6) in the Fig. 1-8.
3. Remove the three stud screws (5) and remove the SW board.

### 1.2.4 Removal of MA board

**Note**

It is not necessary to remove the MA board for checking of solded side of the MA board.
To see soldered side of the board, remove the six screws (7) in the Fig. 1-9 and remove the bottom cover.

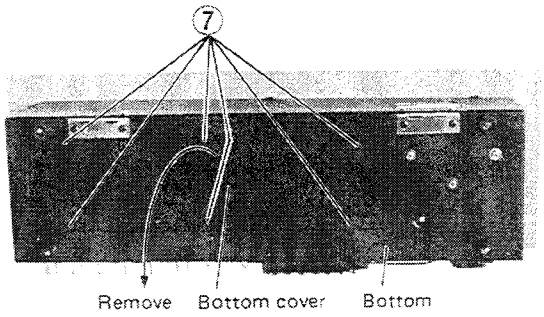



Fig. 1-9

1. Remove the flat cables (F), (G).
2. Remove the connectors (H), (I), (J).
3. Remove the six screws (8) and remove the MA board.

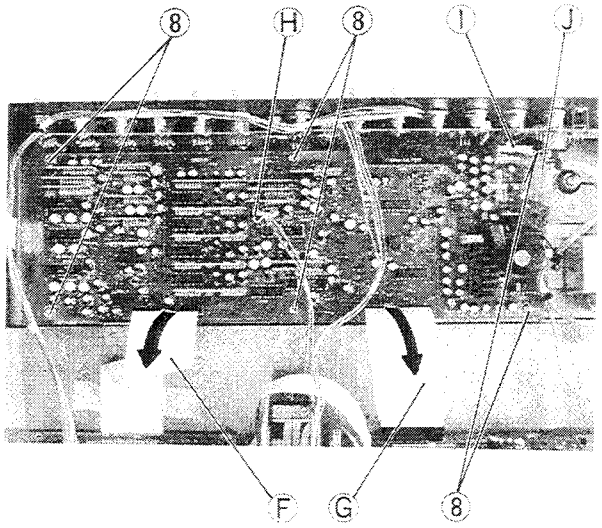



Fig. 1-10

### 1.2.5 Removal of fader ass'y

- Open the control panel according to 1.2.1.

1. Remove the flat cable (K) in the Fig. 1-11.

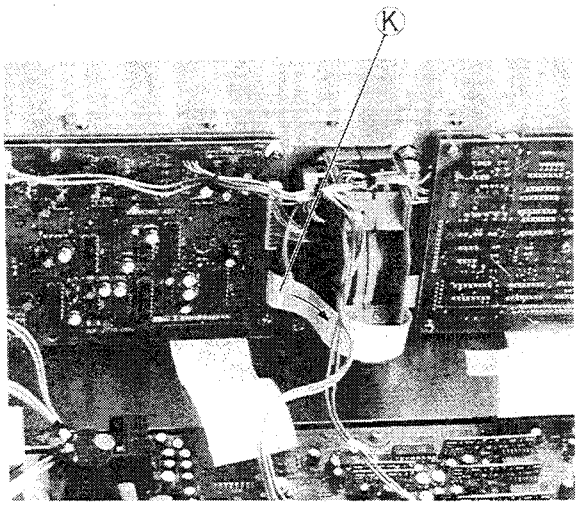



Fig. 1-11

2. Remove the two plate on the fader lever in the Fig. 1-12 by screw driver (blat type) etc.
3. Remove the screws under the plate and take out the fader ass'y.

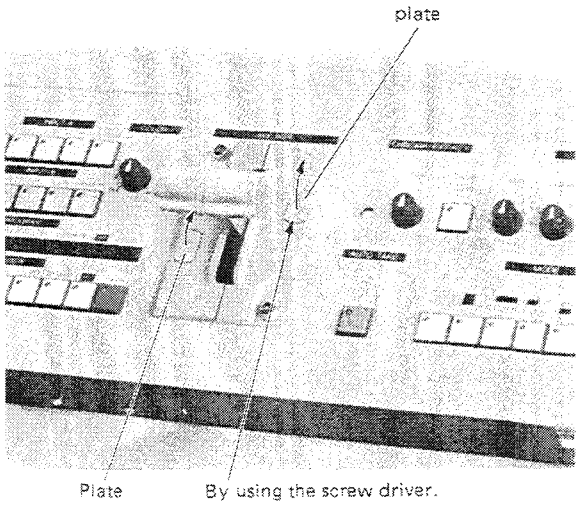



Fig. 1-12

### 1.2.6 Removal of FADER VR

1. Remove the two screws (9) and pull the VR backward.

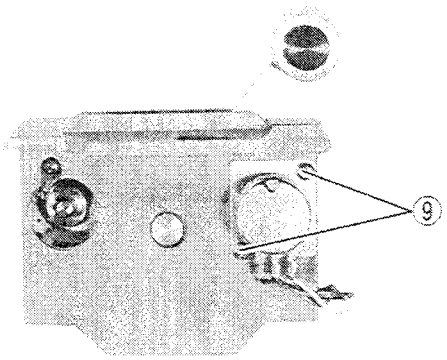



Fig. 1-13

2. Loowen the screw (L) with a hex-wrench and remove the gear. Then, loosen the nut M on the VR plate.

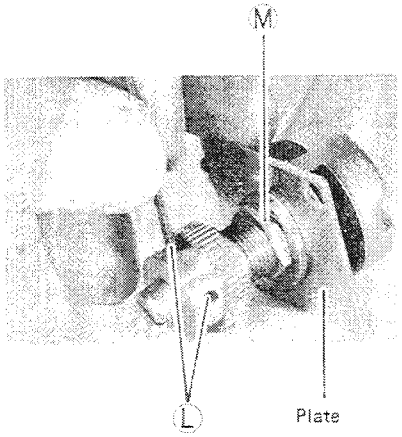



Fig. 1-14

- Adjustment of FADER VR

1. Loosen the two screws (10) with a hex-wrench.

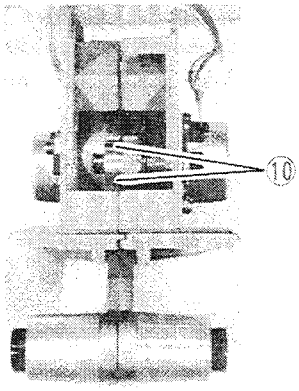



Fig. 1-15

2. Adjust the position using a flat balde screwdriver, and fix the VR with a hex-wrench after adjustment.

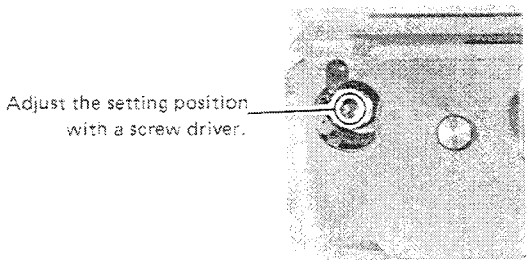
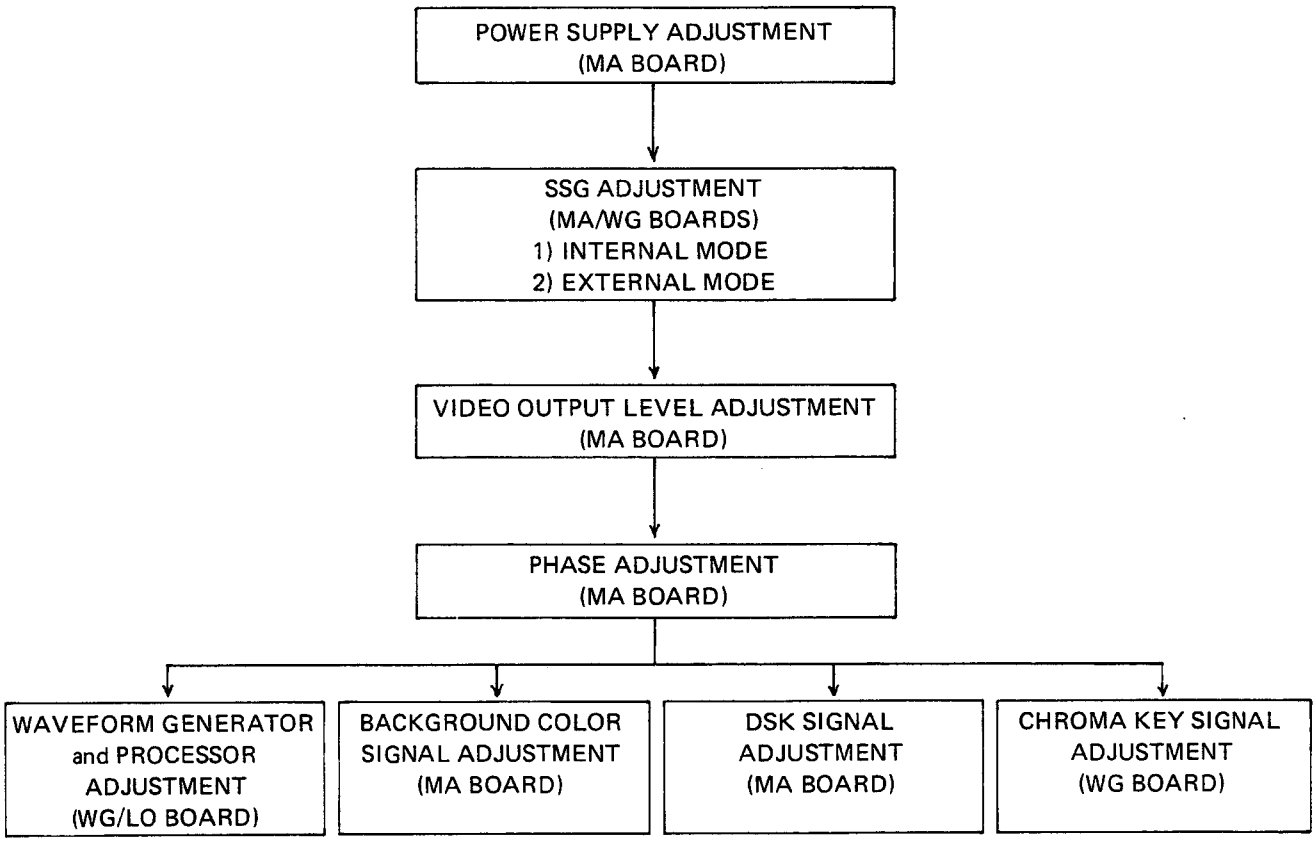



Fig. 1-16

# SECTION 2
# ADJUSTMENTS

■ ADJUSTMENT PROCEDURES




## 2.1 TEST EQUIPMENT AND CONNECTION FOR ADJUSTMENT

- Digital Voltmeter or V.T.V.M.
- Dual Trace Oscilloscope (Tektronix 465B, etc.)
- Test Signal Generator (with Color bars, Stair-step Generators)
- Frequency Counter
- Vectorscope (Tektronix 1420, etc.)
- Waveform Monitor (Tektronix 528, etc.)
- Color Monitor (Under-scanning is recommended.)
- Black and White Monitor (Under-scanning is recommended.)
- Extender Cables* (for Servicing) 1) 12-pin (Part No. SCV0693)
  2) 8-pin (Part No. SCV0694)

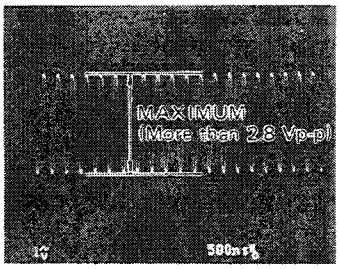
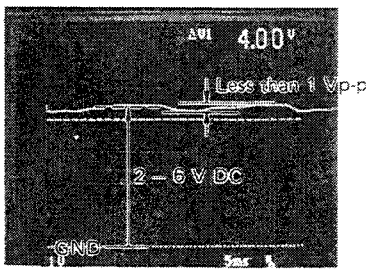
* Cable is used for BY-110 Servicing Jig.

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.2 POWER SUPPLY ADJUSTMENT

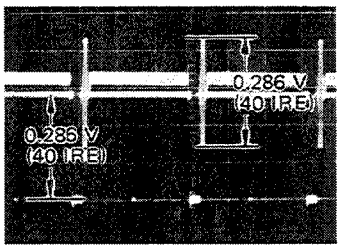
| | | | | |
|---|---|---|---|---|
| 1 | +9 V ADJ. | —<br>Digital Voltmeter | • TP-4 (MA Board)<br>• +9 V ± 0.1 V DC<br>• R270 (+9 V ADJ) (MA Board) | 1) Connect a digital voltmeter + (plus) to TP-4 of the MA Board and — (minus) to chassis.<br>2) Adjust R270 (+9 V ADJ) on the MA Board so that the reading is 9 V. |

## 2.3 SSG ADJUSTMENT (INTERNAL MODE)

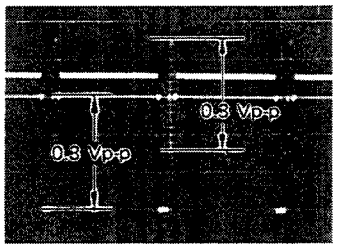
| | | | | |
|---|---|---|---|---|
| 1 | fsc<br>SC FREQ.<br>ADJ. | —<br>Frequency Counter | • TP-5 (MA Board)<br>NTSC / PAL: C43 (SC FREQ) (MA Board): 3.579545 MHz ± 10 Hz / 4.433619 MHz ± 10 Hz | 1) Connect a frequency counter to TP-5 on the MA board.<br>2) NTSC Adjust SC FREQ trimming capacitor (C43) so that the reading is 3.579545 MHz.<br>PAL Adjust SC FREQ trimming capacitor (C43) so that the reading is 4.433619 MHz. |
| 2 | H. OSC<br>SET<br>NTSC | —<br>Digital Voltmeter | • TP-2 (WG Board)<br>• 3.5 ± 0.1 V DC<br>• L6 (H. OSC) (WG Board) | 1) Connect a digital voltmeter + to TP-2 of the WG Board and — to chassis.<br>2) Adjust L6 (H. OSC) so that the reading is 3.5 V. |
| | H. OSC<br>SET<br>PAL | Oscilloscope:<br>H-rate | • IC13-13 pin (WG Board)<br>• Maximum output<br>2.8 Vp-p or more<br>• T2 (fsc-25 Hz)<br>(WG Board) | 1) Connect an oscilloscope to IC13-13 pin on WG board.<br>2) Adjust T2 (H. OSC) transformer so that signal level is maximum.<br>(more than 2.8 Vp-p)<br>  <br><br>Fig. 2-P-1 |
| | | | • TP-3<br>(WG Board)<br>• Ripple : Less than 1 Vp-p<br>Average DC : 2 — 6 V<br>• C123<br>(282 fh)<br>(WG Board) | 1) Connect an oscilloscope to TP-3 with V-rate time division.<br>2) Adjust trimmer capacitor (C123) so that average DC level of waveform is 2 V to 6 V and minimum ripple are observed.<br>  <br><br>Fig. 2-P-2 |

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 3 | BB-1 OUTPUT LEVEL ADJ. | —<br>Oscilloscope:<br>H-rate, 20 μs<br>(75 Ω termination) | • BB-1 OUTPUT | 1) Connect an oscilloscope to BB-1 output terminal (75 Ω termination).<br>2) Adjust R237 (BB-SYNC) and R240 (BB-BURST) so that the signal levels are specified. |

| | NTSC | PAL |
|---|---|---|
| R237<br>BB-SYNC<br>(MA Board) | 0.284 V | 0.3 V |
| R240<br>BB-BURST<br>(MA Board) | 0.284 V | 0.3 V |




NTSC




PAL

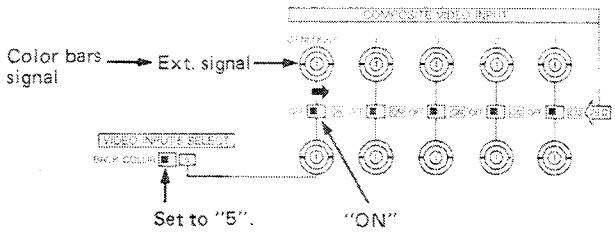
Fig. 2-1

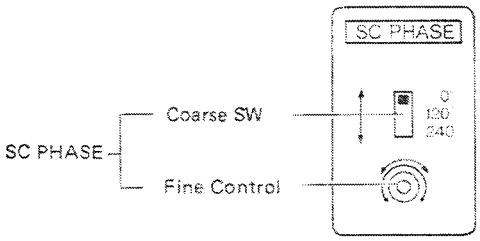
| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.4 SSG ADJUSTMENT (EXTERNAL MODE)

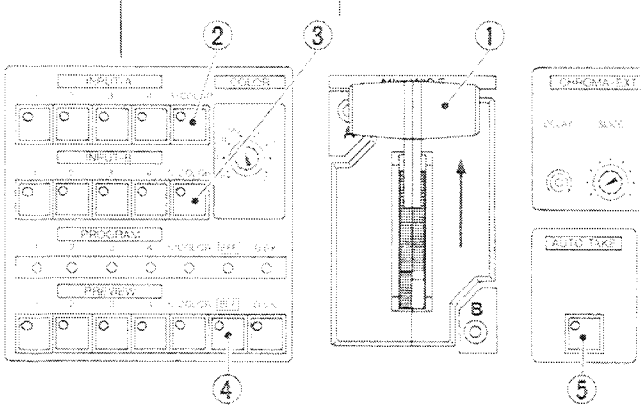
- **Before starting adjustment, proceed as follows.**

1. Apply a color bars signal (1.0 Vp-p) to "GENLOCK/5" INPUT. (EXT. MODE)
2. Set the 75 termination switch to "ON" and VIDEO INPUT 5 SELECT switch to "5".
3. Adjust "SC PHASE" on the front panel. (Refer to INSTRUCTIONS on page 9.)




| | | | | |
|---|---|---|---|---|
| 1 | H. PHASE ADJ. | Color Bars Signal<br>Oscilloscope: H-rate, Delay Mode | • A-ch: GENLOCK/5 (through out)<br>• B-ch: PGM OUTPUT (75 Ω termination)<br>• R29 (H. PHASE)(WG Board) | 1) Connect an oscilloscope A-ch to GENLOCK/5 INPUT and B-ch to PGM-1.<br>2) Press the 5/color buttons of A and B bus-lines.<br>3) Press the EFF button of PREVIEW bus-line, then press "AUTO TAKE" button.<br>4) Set the fader-lever to "A".<br>5) Adjust R29 (H. PHASE) so that H. PHASE timing is equal. |
| 2 | H. Lock ADJ<br>PAL only | –<br>Digital Voltmeter | • TP-2 (WG Board)<br>• 3.5 V ± 0.3 V DC | 1) Connect a digital voltmeter to TP-2 on WG Board.<br>2) Adjust L6 (H LOCK) so that DC level is 3.5 V. |




Setting: Set the lever (1) to "A".
Press the buttons ((2) → (3) → (4) → (5)).

A-ch:

B-ch:

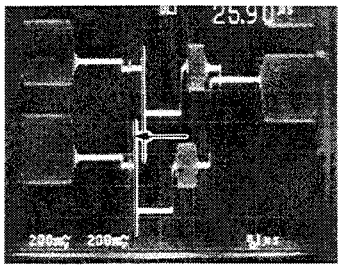
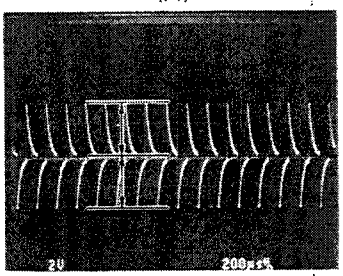


**Fig. 2-2**

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 3 | SC LEVEL ADJ. | Color Bars Signal<br>Oscilloscope: V-rate, 2 msec | →•CN21 pin 1 (WG Board)<br>• T1 (SC LEVEL) (WG Board) | 1) Connect an oscilloscope to pin 1 of CN21.<br>2) Adjust T1 so that SC level is maximum. |
| 4 | SC LOCK ADJ.<br>NTSC | Color Bars Signal<br>Oscilloscope: V-rate, AC | →•TP-1 (WG Board)<br>• R62 (SC LOCK) (WG Board) | 1) Connect an oscilloscope to TP-1 on WB board.<br>2) Adjust R62 (SC LOCK) so that the SC p-p level is minimized. |
| 5 | SC LOCK ADJ<br>PAL | Color Bars Signal<br>Oscilloscope: V-rate, AC | →• TP-1 (WG Board)<br>• R62 (SC LOCK) (WG Board) | 1) Connect an oscilloscope to TP-1 with V-rate time division.<br>2) Adjust R62 (SC LOCK) so that waveform become (A) condition as Fig. 2-P-3. |

(A)



(B)

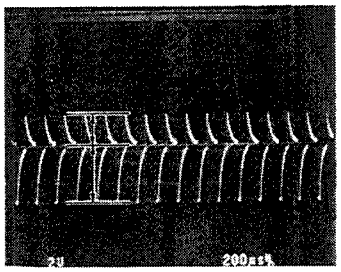


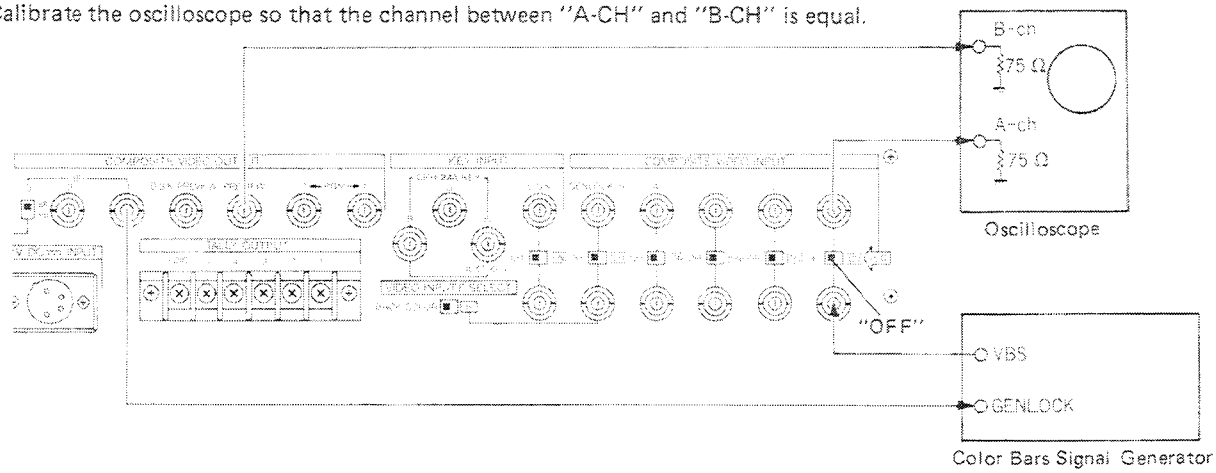
Fig. 2-P-3

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

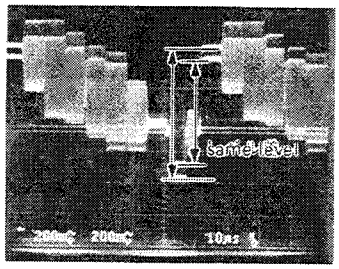
## 2.5 VIDEO OUTPUT LEVEL ADJUSTMENT

- **Before starting adjustment, connect the unit as shown below.**

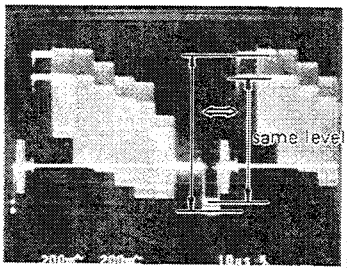
1. Adjust the horizontal phase and SC phase for "INPUT 1". (Refer to INSTRUCTIONS on page 5, System Adjustment.)
2. Calibrate the oscilloscope so that the channel between "A-CH" and "B-CH" is equal.




| | | | | |
|---|---|---|---|---|
| 1 | PREVIEW OUTPUT GAIN ADJ. (1 to 5/Color) | Color Bars Signal (1.0 Vp-p) Oscilloscope: H-rate, 10 μs (75 Ω termination) | A-ch: INPUT 1 (through out) B-ch: PREVIEW OUTPUT • R78 (PVW GAIN) (MA Board) | 1) Press the PREVIEW-Bus button "1". 2) Adjust R78 (PVW GAIN) so that ratio between A-ch and B-ch of oscilloscope is 1:1 (1.0 Vp-p). |
| 2 | PREVIEW OUTPUT GAIN ADJ. (EFF) | • Measuring condition is the same as above. | • R36 (A-GAIN) (MA Board) • R34 (B-GAIN) (MA Board) | 1) Press the MODE SELECT button. 2) Press "1" button of A and B bus lines. 3) Press "EFF" button of PREVIEW bus line. 4) Set the FADER lever to "A" side and adjust R36 (A-GAIN) so that ratio between A-ch and B-ch of oscilloscope is 1 : 1 (1.0 Vp-p). 5) Set the FADER lever to "B" side and adjust R34 (B-GAIN) so that the ratio is 1 : 1. |

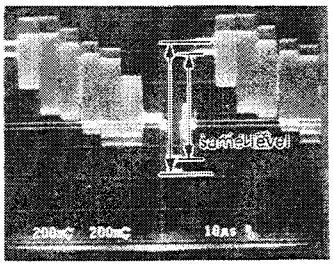



NTSC

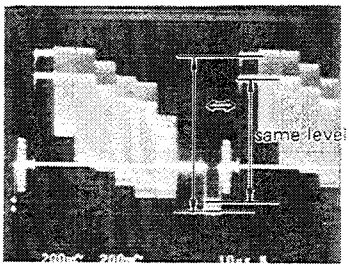



PAL

Fig. 2-3



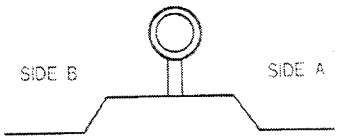

NTSC




PAL

Fig. 2-4

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 3 | PREVIEW OUTPUT PEDESTAL ADJ. (EFF) | — Oscilloscope: H-rate, 10 μs | PREVIEW OUTPUT<br>• R22 (B-PEDESTAL) (MA Board) | 1) Connect an oscilloscope to PREVIEW OUTPUT (no termination).<br>2) Press the MODE SELECT button ■.<br>3) Select the COLOR SELECT switch to "BLK" (BLACK).<br>4) Press the 5/COLOR button of A and B bus lines.<br>5) Press "EFF" button of PREVIEW bus line.<br>6) Set the FADER lever to center position.<br>7) Adjust R22 (B-PEDESTAL) so that A and B bus signals are the same level at the wipe edge. |
| 4 | WIPE EDGE ADJ. | • Measuring condition is the same as above. | • R26 (DIF BAL) (MA Board) | 8) Connect a monitor TV set to PREVIEW OUTPUT.<br>9) Select the MODE ●.<br>10) Adjust R26 (DIF BAL) so that wipe edge is disappear on the monitor.<br>11) Repeat the adjustment No. 2 (Item: PREVIEW OUTPUT GAIN ADJ. [EFF]). |



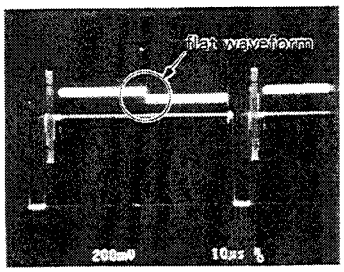




Fig. 2-5

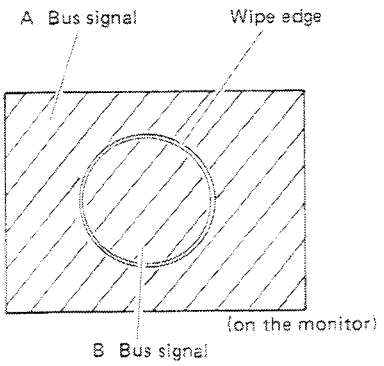
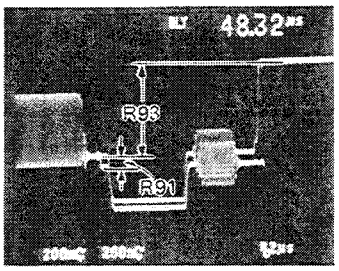
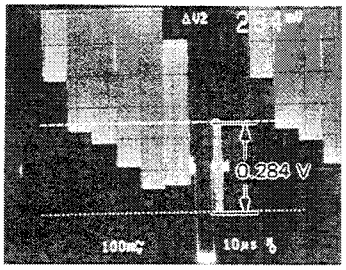
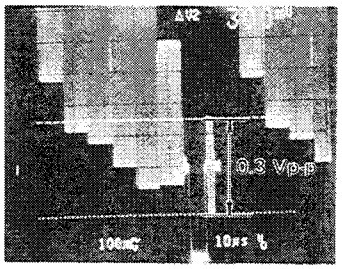
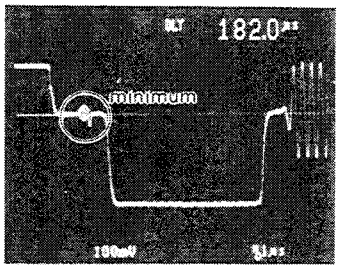
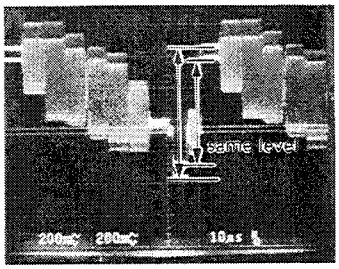
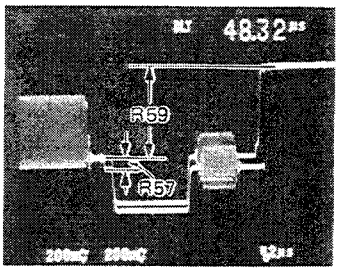
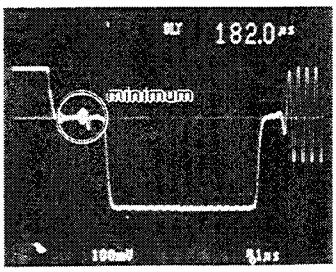



Fig. 2-6

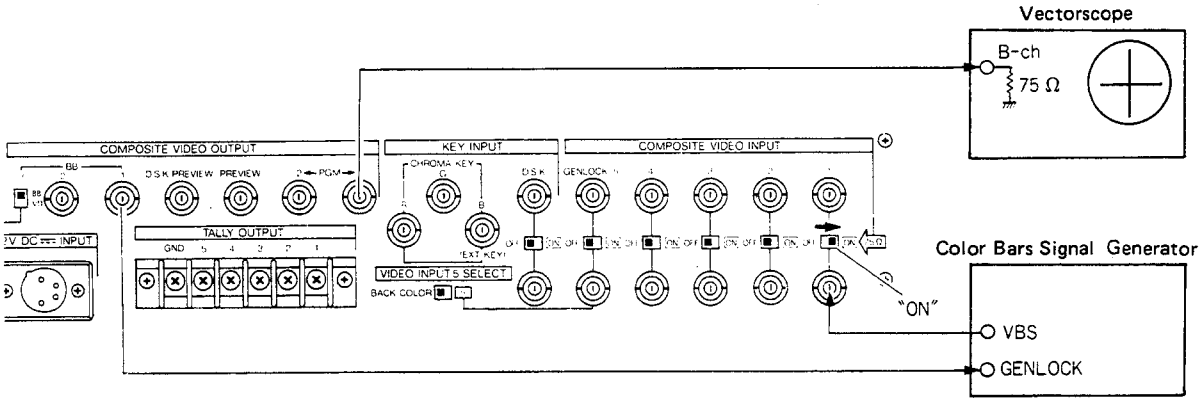
| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 5 | PROGRAM OUTPUT GAIN ADJ. (EFF) | Color Bars Signal (1.0 Vp-p)<br>Oscilloscope: H-rate, 10 μs (75 Ω termination) | A-ch: INPUT 1 (through out)<br>B-ch: PGM-1 OUTPUT (output)<br>• R93 (PGM-1 GAIN) (MA Board)<br>• R91 (DSK-PED)(MA Board) | 1) Connect an oscilloscope B-ch to PGM-1 OUTPUT and A-ch to INPUT 1.<br>2) Press "1" buttons of A and B bus lines.<br>3) Press "EFF" button of PREVIEW bus line.<br>4) Press "AUTO TAKE" button.<br>5) Set the FADER lever to "A" side.<br>6) Adjust R93 (PGM-1 GAIN) so that A-ch and B-ch signal levels (pedestal to white peak) are the same.<br>At the same time, adjust R91 (DSK-PED) so that A-ch and B-ch signals are the same. |
| | | | |  <br>Fig. 2-7 |
| | | | • R192 (DSK CHROMA) (MA Board) | 7) Adjust R192 (DSK-PED) so that the burst level is specified. |
| | | | |  <br>NTSC<br>  <br>PAL<br>Fig. 2-8 |
| | | | • R74 (DIF BAL) (MA Board) | 8) Adjust R74 (DIF BAL) so that noise of front porch is minimum at the B-ch. |
| | | | |  <br>Fig. 2-9 |

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 6 | PROGRAM OUTPUT GAIN ADJ. (1 to 5/ COLOR) | • **Measuring condition is the same as the adjustment before.** | • R69 (PGM-2 GAIN) (MA Board) | 9) Press "1" button of PREVIEW bus line.<br>10) Press "AUTO TAKE" button.<br>11) Adjust R69 (PGM-2 GAIN) so that A-ch and B-ch signals are the same (1.0 Vp-p).<br>  <br><br>Fig. 2-10 |
| 7 | DSK PREVIEW GAIN ADJ. | • **Measuring condition is the same as the adjustment before.** | • R59 (D. PV-GAIN) (MA Board)<br>• R57 (D. PV-PED) (MA Board) | 12) Connect an oscilloscope to PREVIEW OUTPUT.<br>13) Press "DSK" button of PREVIEW but line.<br>14) Set the "DSK LEVEL" and "DSK SLICE" potentiometer to counterclockwise position (on the front panel).<br>15) Adjust R59 (D. PV-GAIN) so that A-ch and B-ch signal levels (pedestal to white peak) are the same.<br>At the same time, adjust R57 (D. PV-PED) so that A-ch and B-ch signals are the same.<br>  <br><br>Fig. 2-11 |
| | | | • R51 (DIF BAL)(MA Board) | 16) Adjust R51 (DIF BAL) so that noise of front-porch is minimized at the B-ch.<br>  <br><br>Fig. 2-12 |

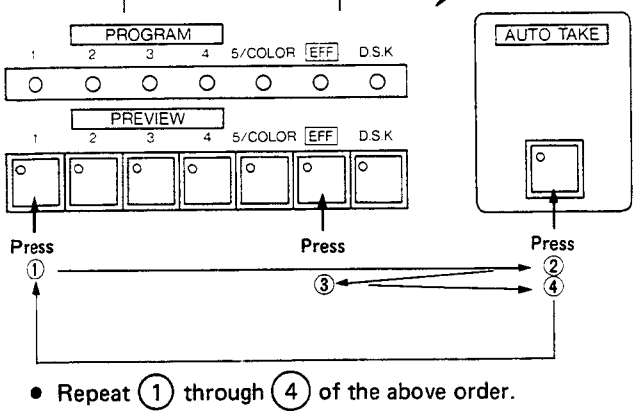
| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.6 CHROMA PHASE ADJUSTMENT

- **Before starting adjustments, connect the unit as shown below.**




| | | | | |
|---|---|---|---|---|
| 1 | PHASE ADJ. (A-Bus ⟷ B-Bus) | Color Bars Signal (1.0 Vp-p) Vectorscope | → • PGM-1 (OUTPUT)<br>• R20 (B-PHASE)(MA Board) | 1) Press "1" buttons of A and B bus lines.<br>2) Press "EFF" button of PREVIEW but line.<br>3) Press "AUTO TAKE" button.<br>4) Select the MODE [MIX].<br>5) When select the FADER lever between A-side to B-side, adjust R20 (B-PHASE) so that color dots of the PGM-1 OUTPUT signal is not changed at the vectorscope. |
| 2 | PHASE ADJ. (A-Bus ⟷ PGM) | • **Measuring condition is the same as above.** | | 6) Set the FADER lever to "A" side.<br>7) Output "1" and "EFF" signals to PGM-1 OUTPUT alternately. (as shown in picture below)<br>At this time, adjust R62 (PGM PHASE) so that color dots of the PGM-1 OUTPUT signal is not changed at the vectorscope. |

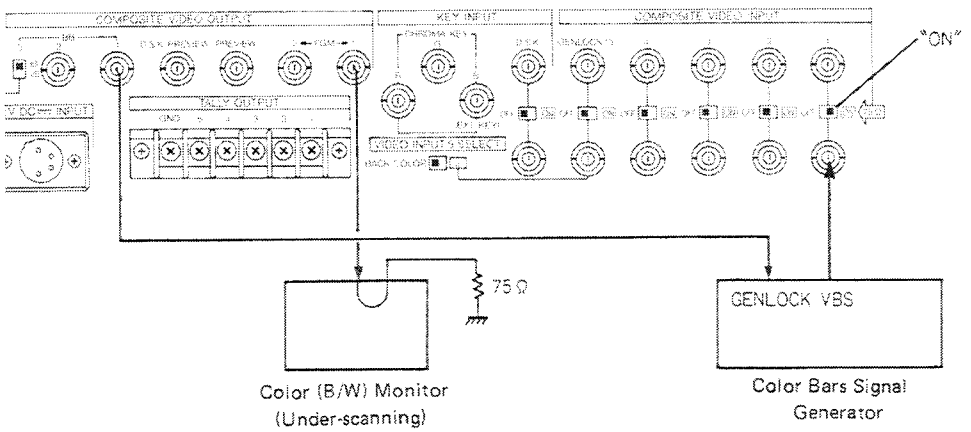


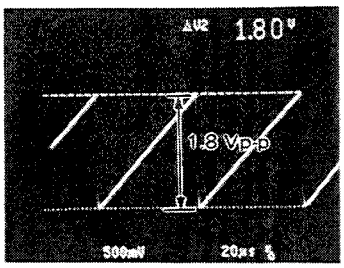

• Repeat (1) through (4) of the above order.

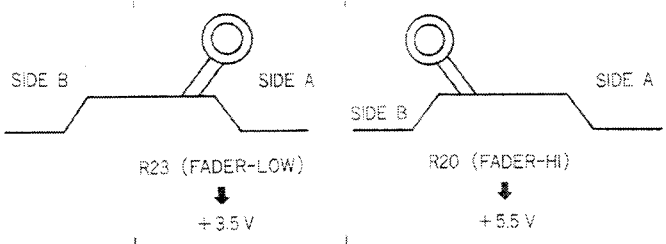
| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.7 WAVEFORM GENERATOR AND PROCESSOR ADJUSTMENT

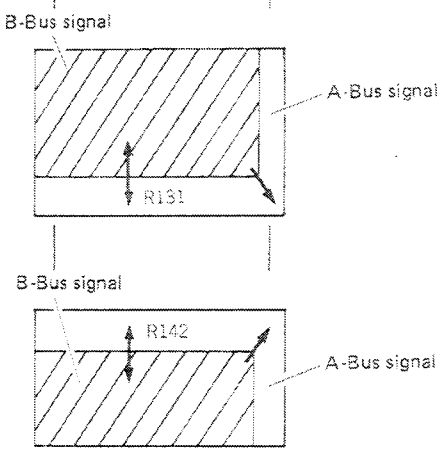
- INPUT SIGNAL (Color bars signal, etc.) is necessary for Adjustments No. 3, 4 and 5.

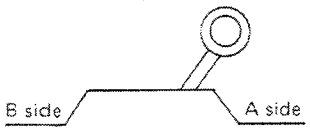


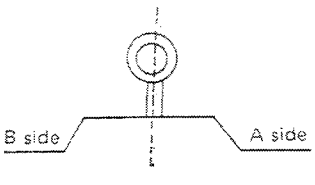

| | | | | |
|---|---|---|---|---|
| 1 | H. SAW LEVEL ADJ. | — Oscilloscope: H-rate, 20 μs | → • TP-4 (WG Board)<br>• 1.8 V ± 0.1 Vp-p<br>• R102 (H-SAW-LEVEL) (WG Board) | 1) Connect an oscilloscope to TP-4.<br>2) Select the WIPE MODE ■□.<br>3) Adjust R102 (H-SAW-LEVEL) so that the signal level is 1.8 Vp-p.<br>  <br><br>Fig. 2-13 |
| 2 | H. WIPE ADJ. | — Digital Voltmeter | → • CN-4 pin 2 (LO Board)<br>• R23 (FADER-LOW) (LO Board)<br>• R20 (FADER-HI) (LO Board) | 1) Press "1" button of A bus-line.<br>2) Press "5/COLOR" of B bus-line.<br>3) Press "EFF" button of PREVIEW bus-line.<br>4) Press "AUTO TAKE" button.<br>5) Select the WIPE ■□.<br>6) Connect a digital voltmeter to CN4 pin 2.<br>7) Set the FADER lever to "A" side and adjust R23 (FADER-LOW) so that the voltage is 3.5 V.<br>8) Set the FADER lever to "B" side and adjust R20 (FADER-HI) so that the voltage is 5.5 V. |



| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 3 | CORNER WIPE ADJ. | Color Bars Signal<br>B/W (Color) Monitor TV (Under-scanning) | • PGM-1 OUTPUT<br>• R131 (V-SAW-LEVEL)<br>• R142 (INV-DC)<br>(WG Board) | 1) Press the "1" button of A bus-line.<br>2) Press the "5/COLOR" button of B bus-line.<br>3) Select the BACK COLOR without BLK (BLACK).<br>4) Press the "EFF" button of PREVIEW bus-line.<br>5) Press the "AUTO TAKE" button.<br>6) Select the WIPE MODE.<br>7) Slide the FADER lever (A ⟷ B) and adjust R131 (V-SAW-LEVEL) so that the wipe finishes H and V together.<br>8) Select the WIPE.<br>9) Slide the FADER lever (B ⟷ A) and adjust R142 (INV-DC) so that the wipe finishes H and V together. |
| 4 | FADER LEVER ADJ. (MIX MODE) | Color Bars Signal<br>Oscilloscope: H-rate, 10 μs | • PGM-1 OUTPUT<br>• R156 (MIX-DC) (WG Board) | 1) Connect an oscilloscope to PGM-1 OUTPUT (75 Ω termination).<br>2) Select MODE MIX button.<br>3) Press "1" button of A bus-line.<br>4) Press "5/COLOR" button of B bus-line.<br>5) Select the BACK COLOR select switch to "BLK" (BLACK).<br>6) Press "EFF" button of PREVIEW bus-line.<br>7) Press "AUTO TAKE" button.<br>8) Set the FADER lever to center position as in Fig. 2-14.<br>9) Adjust R156 (MIX-DC) so that white peak level of the color bars signal becomes half level. |



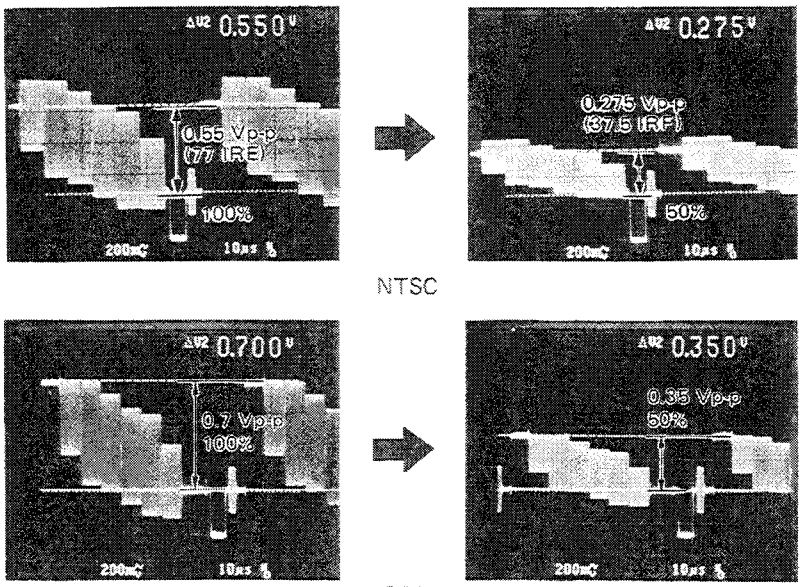
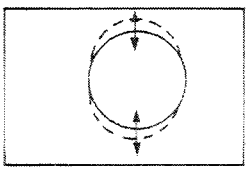
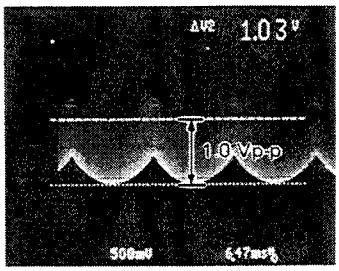
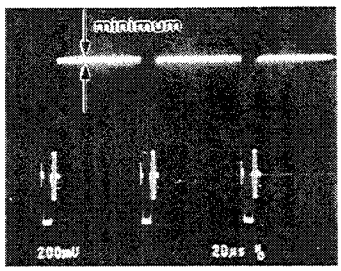
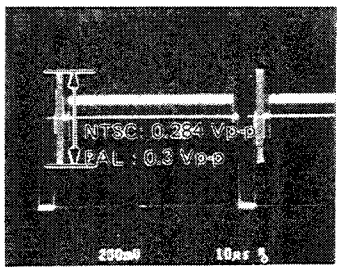




Fig. 2-14

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|
| 5 | CIRCLE WIPE ADJ. | • **Measuring condition is the same as before.**<br>Oscilloscope: V-rate, 5 ms → • TP-4 (WG Board)<br>• 1.0 Vp-p<br>• R107 (H-PARA-LEVEL) (WG Board)<br>B/W (Color) Monitor TV → • PGM-1 OUTPUT<br>• R136 (V-PARA-LEVEL) (WG Board)<br>  <br>(monitor picture) | 1) Select WIPE [●].<br>2) Connect an oscilloscope to TP-4.<br>3) Adjust R107 (H-PARA-LEVEL) so that signal amplitude is 1.0 Vp-p.<br>  <br>Fig. 2-15<br>4) Press the "1" button of A bus-line.<br>5) Press the "5/COLOR" button of B bus-line.<br>6) Select the BACK COLOR without BLK (BLACK).<br>7) Press the "EFF" button of PREVIEW bus-line and press "AUTO TAKE" button.<br>8) Connect a monitor to PGM-1 OUTPUT.<br>9) Adjust R136 (V-PARA-LEVEL) so that wipe pattern becomes circle on the monitor. (Slide the FADER lever.) |

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.8 BACK COLOR ADJUSTMENT

| | | | | |
|---|---|---|---|---|
| 1 | BACK COLOR WHITE-BALANCE ADJ. | — Oscilloscope: H-rate, 10 μs | • PGM-1 OUTPUT<br>• R105 (BC-W-BAL) (MA Board) | 1) Connect an oscilloscope to PGM-1 OUTPUT (75 Ω termination).<br>2) Press "5/COLOR" buttons of each bus-line.<br>3) Press "AUTO TAKE" button.<br>4) Set the FADER lever to "A" side.<br>5) Select the BACK COLOR select switch to "W" (WHITE).<br>6) Adjust R105 (BC-W-BAL) so that the carrier leakage of white peak level is minimized.<br>  <br>Fig. 2-16 |
| 2 | BACK COLOR PHASE ADJ. | — Vectorscope | • PGM-1 OUTPUT<br>• C111 (QUAD PHASE)<br>• R295 (BC PHASE) (MA Board)<br>10°/10% | 1) Connect a vectorscope to PGM-1 OUTPUT.<br>2) Press "5/COLOR" buttons of each bus-line.<br>3) Set the FADER lever to "A" side.<br>4) Press AUTO TAKE" button.<br>5) Adjust C111 (QUAD PHASE) and R295 (BC-PHASE) alternately and repeatedly so that all of the spots (B, R, MG, G, CY, Y) will be in their specified positions on the vectorscope by selecting the BACK COLOR select switch. |
| 3 | BACK COLOR CHROMA LEVEL ADJ. | — Oscilloscope: H-rate, 10 μs | • PREVIEW OUTPUT<br>• R131 (BC CHROMA) (MA Board)<br> <br> | 1) Connect an oscilloscope to PREVIEW OUTPUT.<br>2) Adjust R131 (BC CHROMA) so that burst level is specified level.<br>  <br><br>Fig. 2-17 |

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.9 DSK COLOR ADJUSTMENT

| | | | | |
|---|---|---|---|---|
| 1 | DSK WHITE-BALANCE ADJ. | – Oscilloscope: H-rate, 10 μs | → • PGM-1 OUTPUT<br>• R162 (DSK-W-BAL) (MA Board) | 1) Connect an oscilloscope to PGM-1 OUTPUT.<br>2) Press "1" buttons of each bus-line.<br>3) Set the FADER lever to "A" side.<br>4) Press "EFF" button of PREVIEW but-line.<br>5) Press "AUTO TAKE" button.<br>6) Select the DSK COLOR select switch to "W" (WHITE).<br>7) Turn the DSK SLICE and LEVEL knobs to clockwise position.<br>8) Set the DSK ON/OFF button to ON.<br>9) Adjust R162 (DSK-W-BAL) so that carrier leakage of white peak level is minimized. |

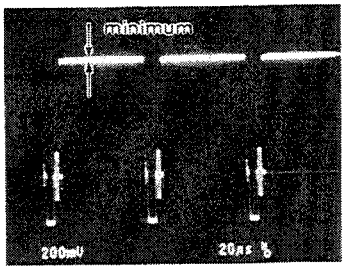
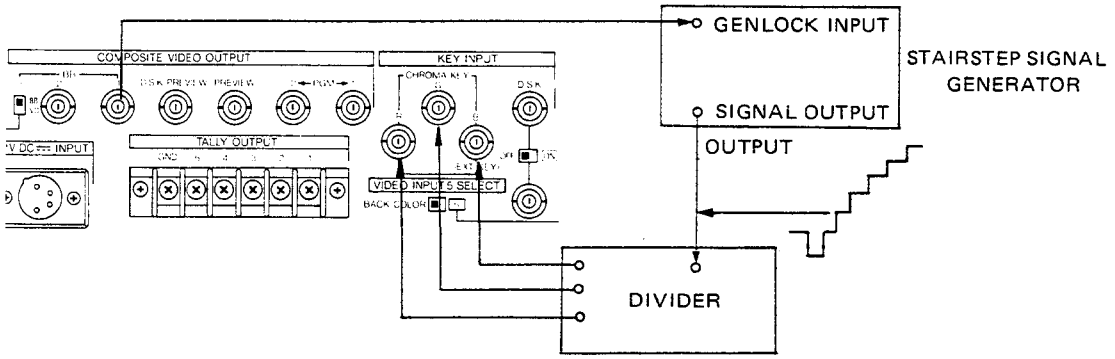



Fig. 2-18

| No. | Item | Measuring Instruments | Measuring Points, Adjusting Levels & Adjusting Points | Procedures |
|---|---|---|---|---|

## 2.10 CHROMA KEY ADJUSTMENT

- **Stair-step signal generator (ex. TG-7) and video signal divider (DV-101, etc.) are necessary for this adjustment.**
- **Before starting adjustments, connect the unit as shown below.**




| | | | | |
|---|---|---|---|---|
| 1 | WHITE-BALANCE ADJ. | Stair-step Signal<br>Oscilloscope: → H-rate, 10 μsec | • TP-7 (WG Board)<br>• R168 (W-BAL)(WG Board) | 1) Connect an oscilloscope to TP-7.<br>2) Adjust R168 (W-BAL) so that carrier leakage of waveform is minimized. |

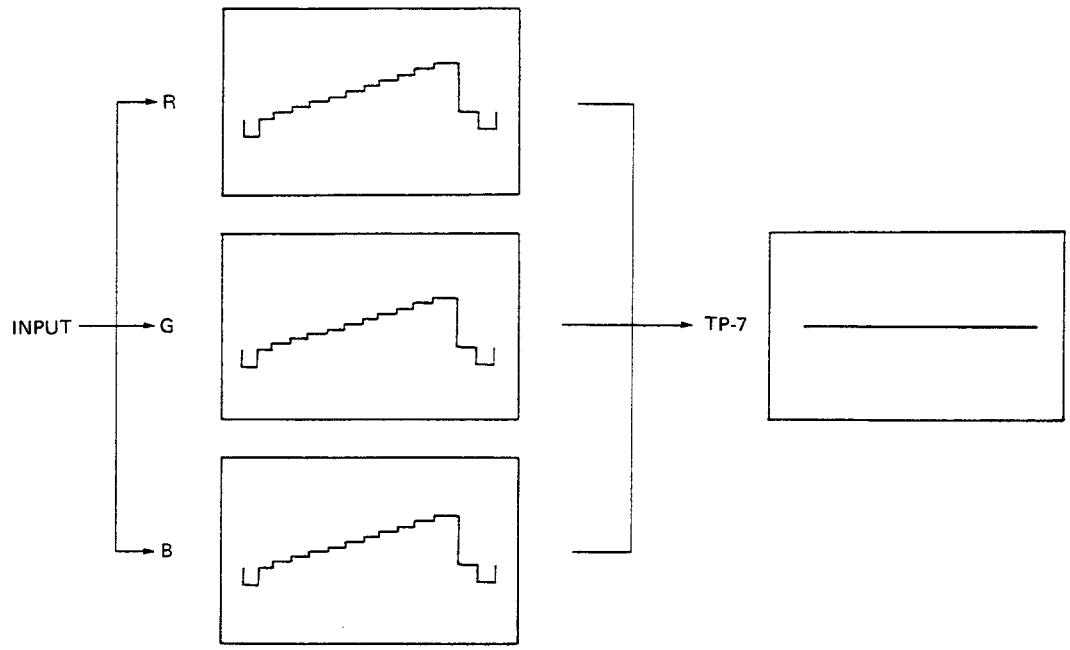
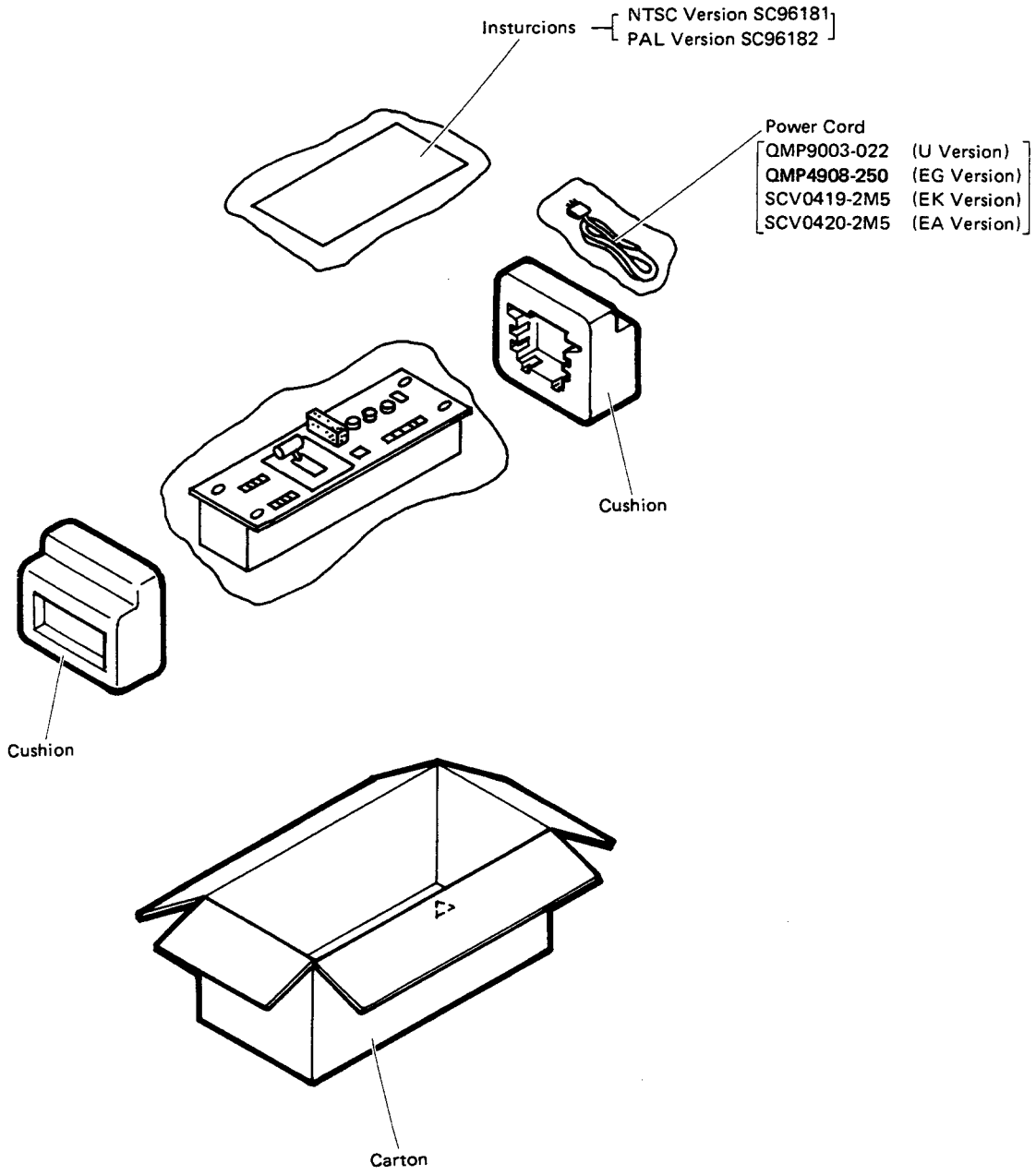



**Fig. 2-19**

# SECTION 3
# REPACKING




"Revised on June 1989"

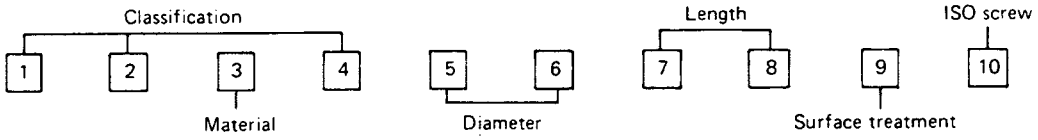
# SECTION 4
# EXPLODED VIEWS AND PARTS LIST

## SAFETY PRECAUTION

**Parts identified by the ⚠ symbol are critical for safety.**
**Replace only with specified part numbers.**

### 4.1 STANDARD PART NUMBER CODING

#### 4.1.1 Screw coding




**Classification** (first digit)

| Symbol Letter | Name |
|---|---|
| S | Normal screw |
| N | Assembly screw |
| L | " |
| D | " |
| M | Wood screw |
| F | Feather screw |
| T | Set screw |
| Y | " |
| B | Bolt |
| N | Nut |
| W | Washer |
| R | E-ring |
| E | Eyelet |
| P | Spring |
| G | Washer head screw |

**Material** (third digit)

| Symbol Letter | Material |
|---|---|
| S | Steel |
| E | Stainless steel |
| C | Cast iron |
| U | Bronze |
| B | Brass |
| P | Phosphor bronze |
| N | German silver |
| Y | Brass |
| A | Aluminum |
| Z | Zinc alloy |
| K | Polycarbonate |

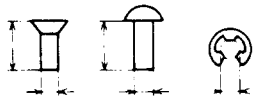
**Shape of Screw Head** (second digit)

| Symbol Letter | | Shape of Screw Head |
|---|---|---|
| P | | Pan head |
| S | | Flat countersunk head |
| H | | Oval countersunk head |
| D | | Binding head |
| R | | Round head |
| B | | Round head |
| T | | Truss head |

**Type of Screw** (fourth digit)

| Symbol Letter | Type of Screw |
|---|---|
| P | Cross-Recessed head screw |
| A | Tapping screw |
| B | Special tapping screw |
| T | Thread rolling tapping screw |
| E | Special tapping screw |
| F | Special tapping screw |

**Diameter and Length of Screw** (fifth – eighth digit)



– Example –
S P B P 3 0 0 6 Z S
(Diameter x 10) (Length)
Diameter : 3 mm
Length : 6 mm

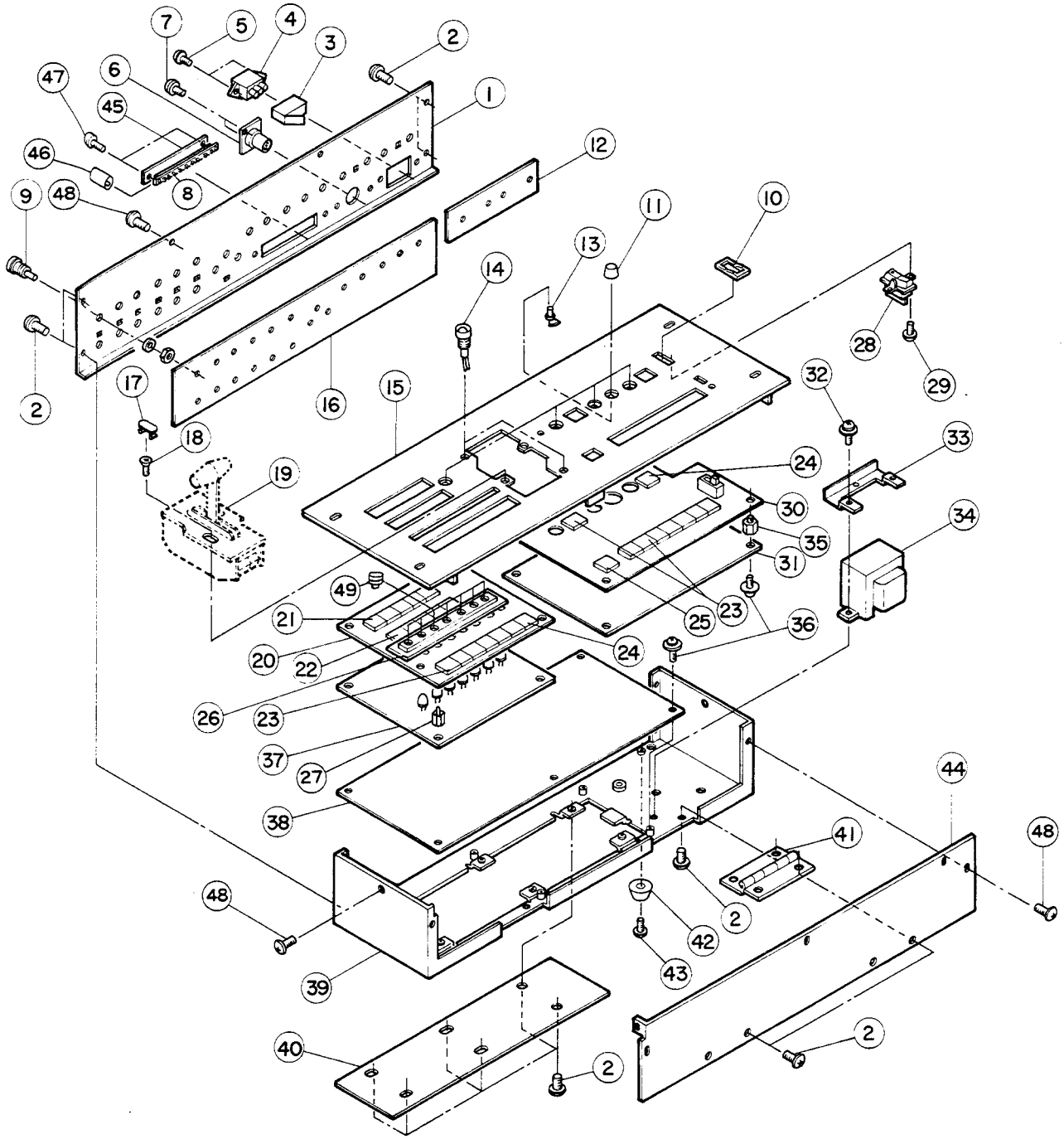
**Surface Treatment** (ninth digit)

| Symbol Letter | Surface Treatment |
|---|---|
| Z | Galvanization, dichromic acid treatment (MFZn2-C) |
| N | Nickel plating (MFNi2, MFNil) |
| R | Chrome plating (MBCr2, MBCr1) |
| G | Silver plating (SP4) |
| W | Nichrome platings |
| P | Phosphite treatment |
| B | Bronze plating |

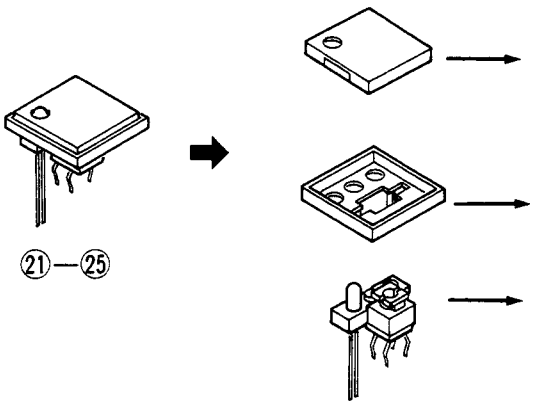
| Symbol letter | Surface treatment |
|---|---|
| M | Black coloring after galvanization |
| A | Red coloring after galvanization |
| C | Blue coloring after galvanization |
| T | Green coloring after galvanization |
| V | Violet coloring after galvanization |
| F | Iron with black coloring |

## 4.2 EXPLODED VIEWS AND PARTS LIST

### 4.2.1 KM-1200 assembly



NOTE: Button switch ( ㉑ , ㉒ , ㉓ , ㉔ , ㉕ ) assembly.



㉑—㉕

| Color | Part No. | Part Name |
|---|---|---|
| Yellow | SCV0748-004 | Cap |
| Orange | " -003 | " |
| White | " -009 | " |
| Brown | " -001 | " |
| Green | " -005 | " |

| | | |
|---|---|---|
| | SCV0747-000 | HOUSING |

| LED | Part No. | Part Name |
|---|---|---|
| Red | SCV0746-002 | LED SW |
| Green | " -005 | " |

KM-1200 assembly list

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| 1 | SC20212-001 | Rear Panel | NTSC |
| | " -002 | " | PAL |
| 2 | SDSP3006M | Screw | M3 x 6 |
| 3 | SCV0801-001 | Cover | |
| 4 | QMC0335-002 | AC Socket | QMCB002-001 EG only |
| 5 | SDSP3008M | Screw | M3 x 8 |
| 6 | GC31917-021 | Connector | XLR 4 Pin |
| 7 | SDSP2006M | Screw | M2 x 6 |
| 8 | SCV750-001 | Terminal Board | |
| 9 | SCV0749-001 | BNC Connector | |
| 10 | SC42025-001 | Switch Guide | |
| 11 | SC41188-004 | Knob | |
| 12 | Not available | BC Board Ass'y | |
| 13 | SC42026-001 | Knob Adapter | |
| 14 | SDB-204B-RDAL | LED | |
| 15 | SC20210-002 | Panel | U/E |
| 16 | Not available | BT Board Ass'y | |
| 17 | SC42028-001 | Cap | |
| 18 | SSSP400€N | Screw | M4 x 6 |
| 19 | — | Fader Lever Ass'y | Refer to 4.2.2 |
| 20 | Not available | SW Board Ass'y | |
| 21 | SC30654-204 | Button SW Ass'y (Yellow) | Refer to Page 4-2 |
| 22 | " -203 | " (Orange) | |
| 23 | " -209 | " (White) | |
| 24 | " -501 | " (Brown) | |
| 25 | " -205 | " (Green) | |
| 26 | SC42027-001 | LED Guide | |
| 27 | SC42031-002 | Stud | |
| 28 | SCV0428-002 | Power Switch | NTSC |
| | SCV0204-002 | " | PAL |
| 29 | LPSP3006Z | Screw | M3 x 6 |
| 30 | Not available | CO Board Ass'y | |
| 31 | " | WG Board Ass'y | |
| 32 | DPSP4008Z | Screw | M4 x 8 |
| 33 | SC42030-001 | Bracket | |
| 34 | SCV0734-002 | Power Trans | 120 V |
| | SCV0735-001 | " | 220/240 V |
| 35 | SC42031-001 | Stud | |
| 36 | DPSP3006Z | Screw | M3 x 6 |
| 37 | Not availabel | LO Board Ass'y | |
| 38 | " | MA Board Ass'y | |
| 39 | SC20215-002 | Chassis | |
| 40 | SC30674-001 | Bottom Cover | |
| 41 | SC40913-002 | Hinge | |
| 42 | QZF1510-001 | Foot | |
| 43 | LPSP3010Z | Screw | M3 x 10 |
| 44 | SC30663-001 | Front Cover | |
| 45 | SC42439-001 | Plate | |
| 46 | SC42440-001 | Stud | |
| 47 | SDSP3020M | Screw | M3 x 20 |
| 48 | DPSP3004N | " | M3 x 4 |
| 49 | SC42450-001 | Lens | |

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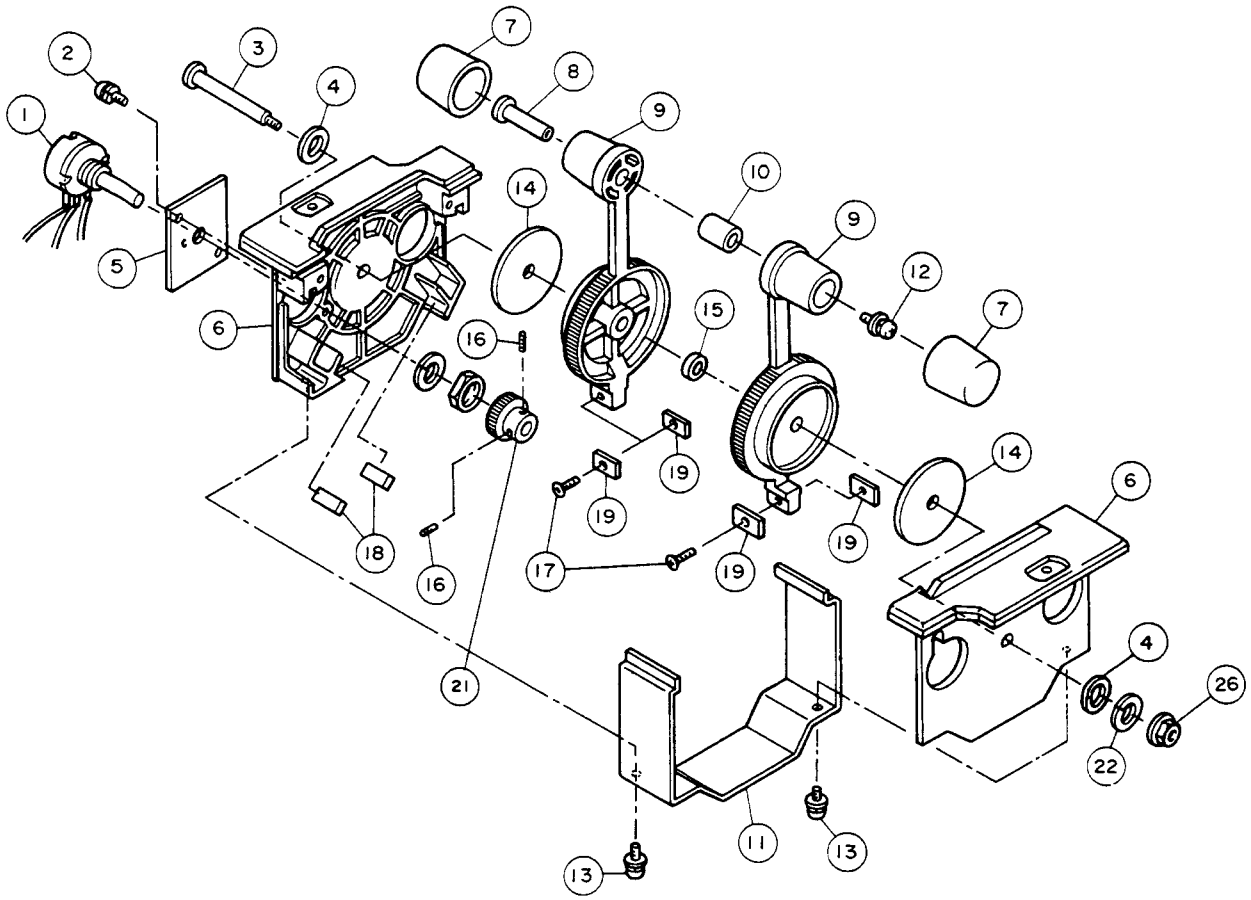
4.2.2 Fader lever assembly

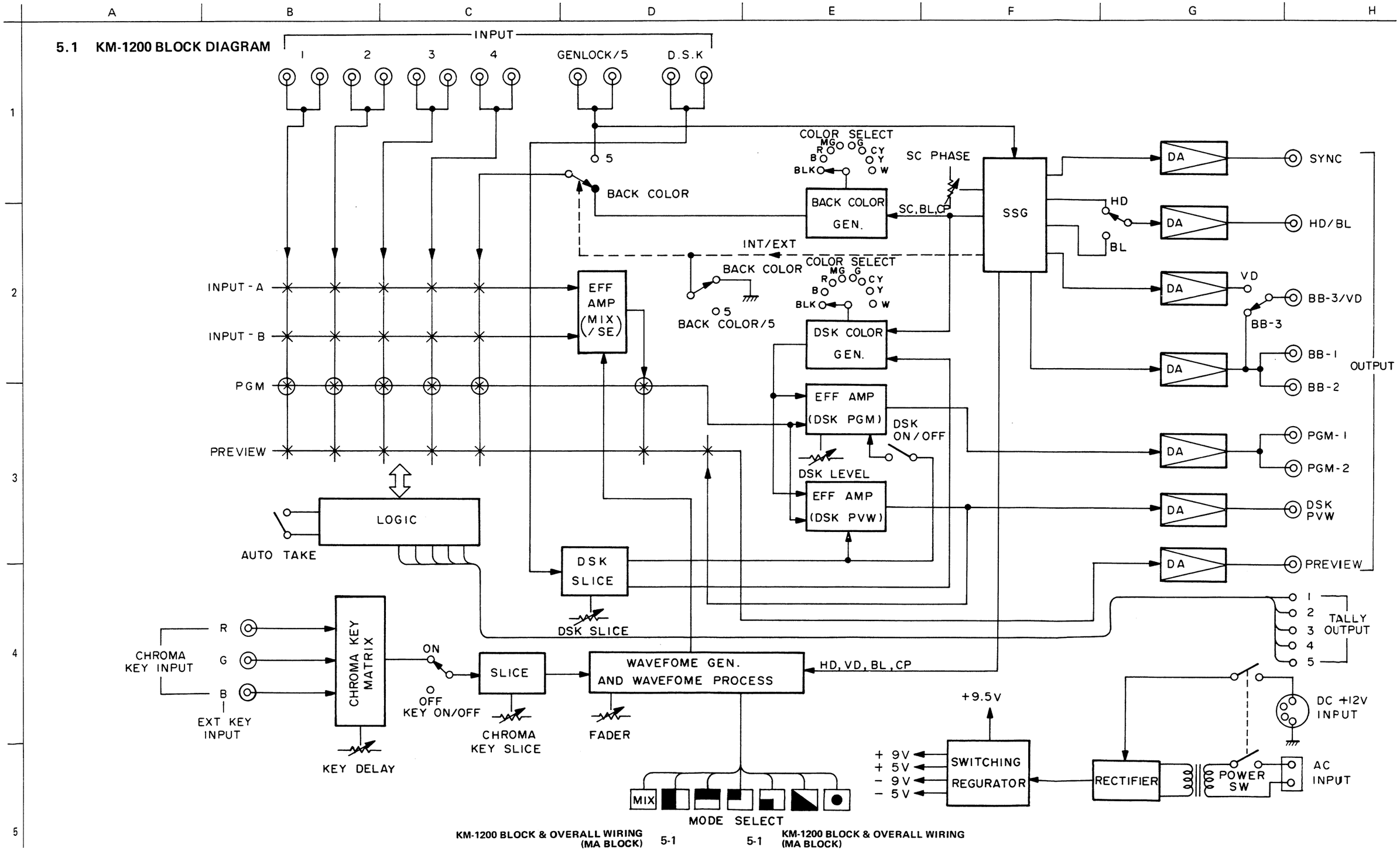


| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| 1 | SCV0289-001 | V. Resistor | 1 kΩ B |
| 2 | SPSP3006Z | Screw | M3 x 6 |
| 3 | SC40708-001 | Spindle | |
| 4 | WNS6000N | Washer | |
| 5 | SC40721-001 | Bracket | |
| 6 | SC20087-002 | Case | |
| 7 | SC42024-001 | Knob Cap | Glued to (9) |
| 8 | SC40727-001 | Shaft | |
| 9 | SC30321-001 | Lever-1 | |
| 10 | SC40728-001 | Sleeve | |
| 11 | SC30327-001 | Cover | |
| 12 | DPSP3006Z | Screw | |
| 13 | LPSP3006Z | " | |
| 14 | SC42419-001 | Sheet | |
| 15 | Q03093-115 | Spacer | |
| 16 | YFS3003F | Set Screw | |
| 17 | SSSP2605N | Screw | |
| 18 | SC40725-001 | M. Rubber | Glued to (6) |
| 19 | SC44085-001 | M. Base | |
| 20 | NFZ5000Z | F. Nut | |
| 21 | SC40713-001 | Gear | |
| 22 | WLS6000M | Washer | |

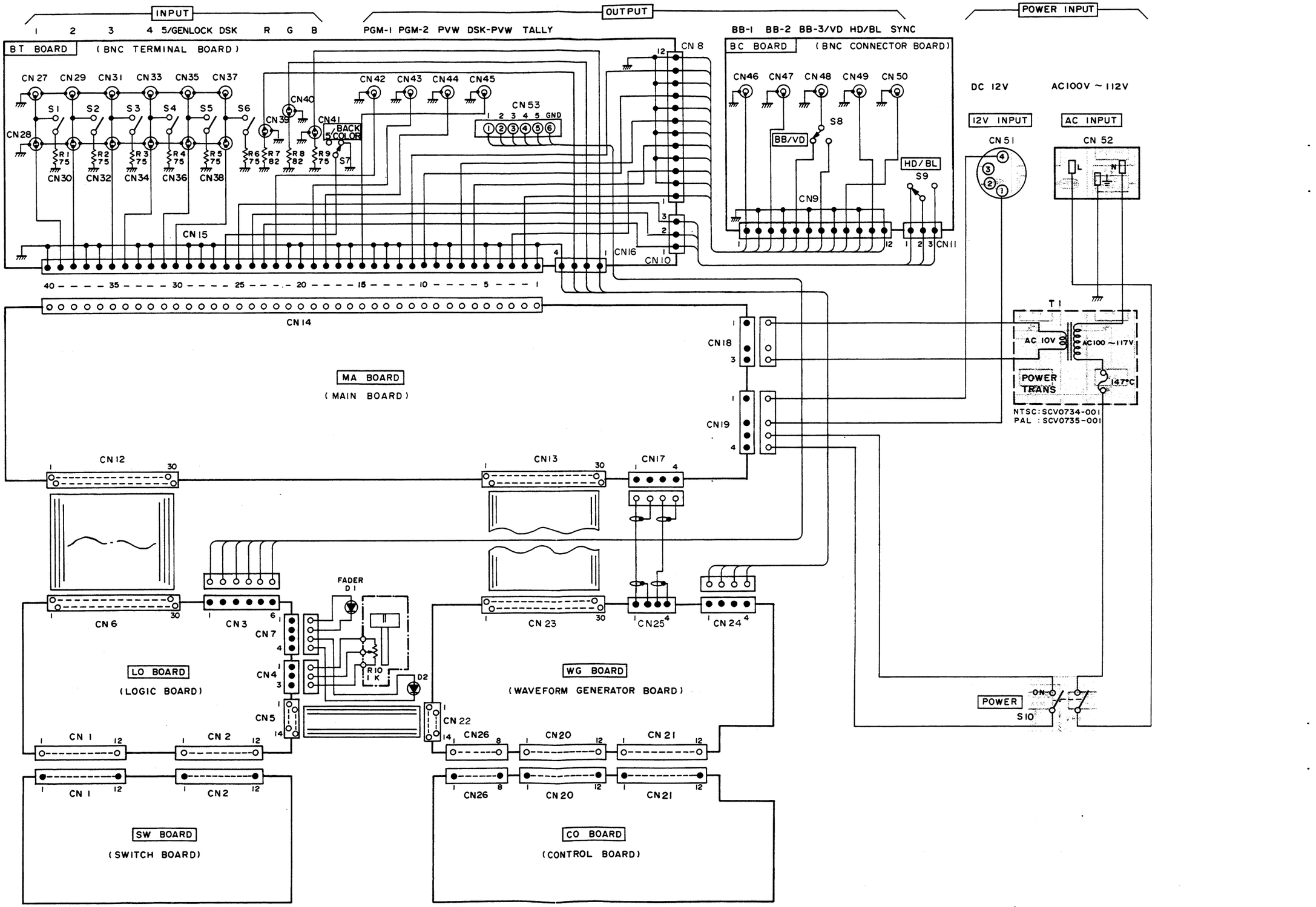
"Revised on June 1989"

# SECTION 5
# CHARTS AND DIAGRAMS

## 5.1 KM-1200 BLOCK DIAGRAM



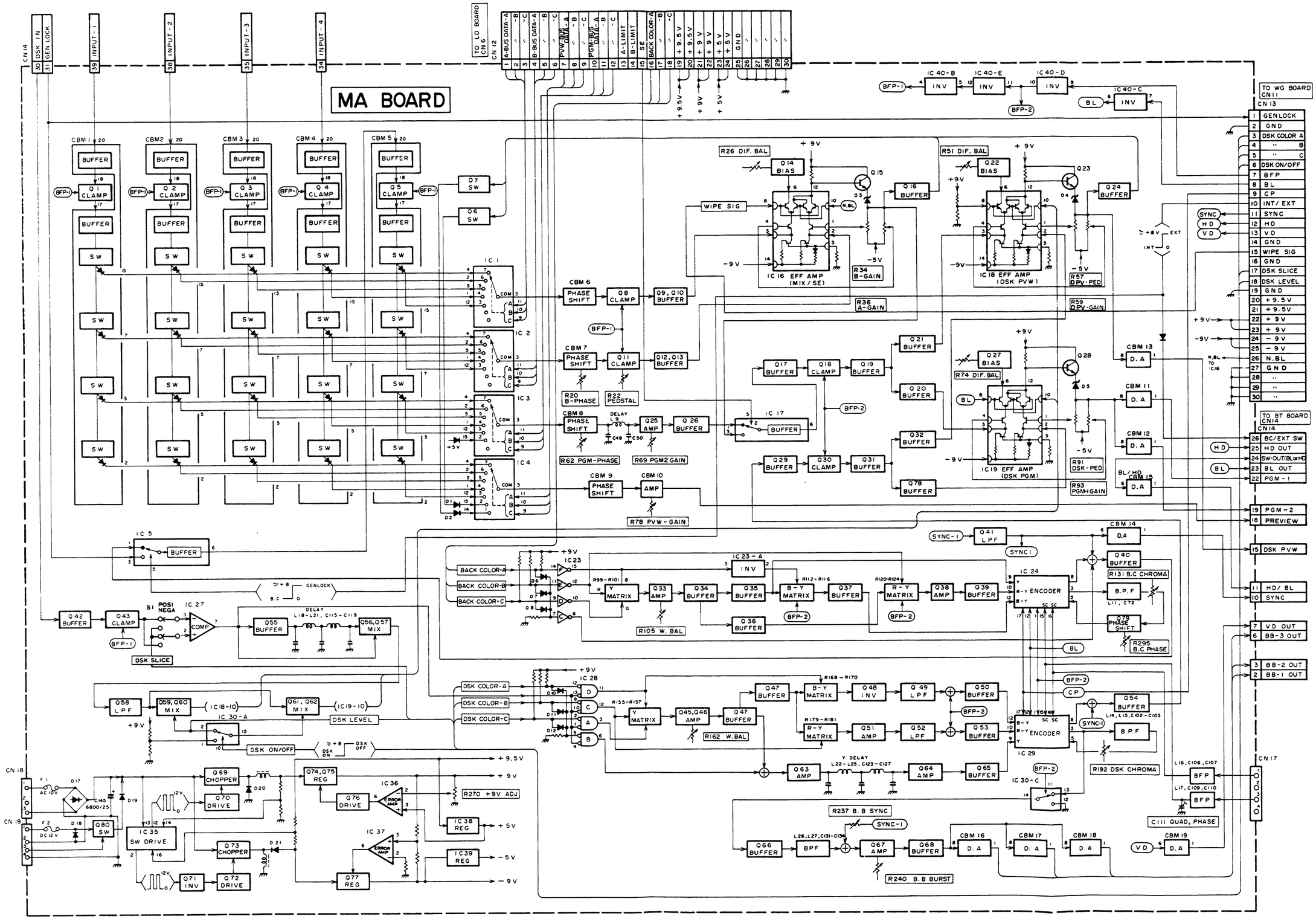
## 5.2 OVERALL WIRINGS






5-1 KM-1200 BLOCK & OVERALL WIRING (MA BLOCK)

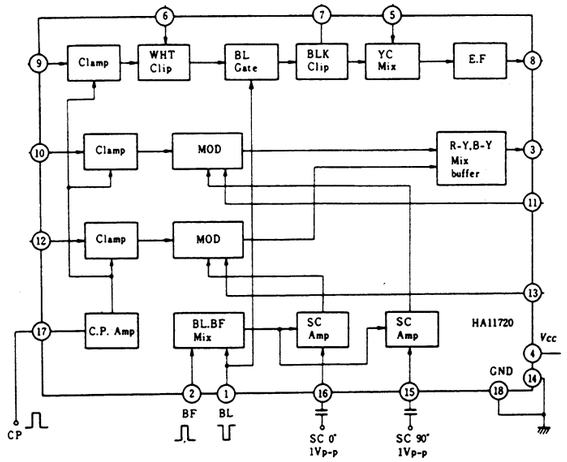
## 5.3 MA BLOCK DIAGRAM



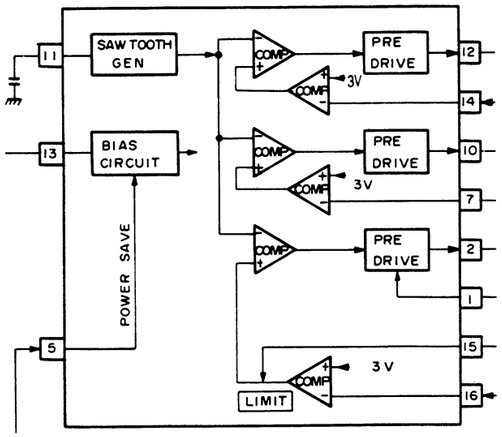



5-2 MA BLOCK (KM-1200 BLOCK & OVERALL WIRING)

## *HA11720 (Encoder) [HITACHI]

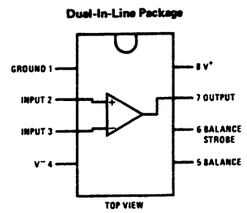



## *HA13002 (DC-DC Converter) [HITACHI]



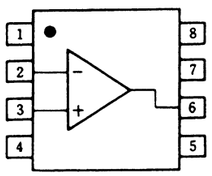

## *LM311 (Volage Comparator) [NATIONAL]

Dual-In-Line Package



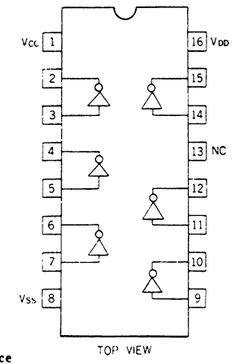

## *NJM5534

(TOP VIEW)

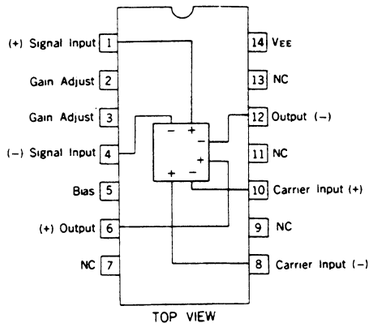


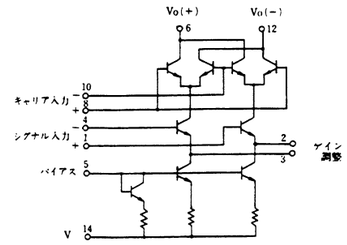
1. Balance
2. −Input
3. +Input
4. V⁻
5. Compensation
6. Output
7. V⁺
8. Balance/Compensation

## *TC4049 (Hex Buffer/Inverter) [TOSHIBA]

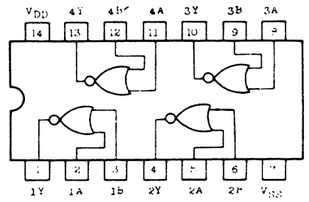



## *NJM1496 (Balance Modulator) [JRC]

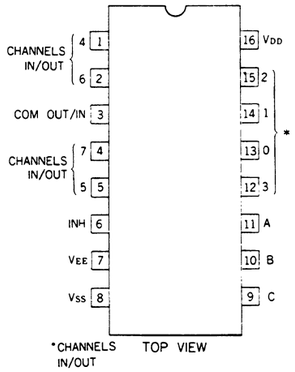


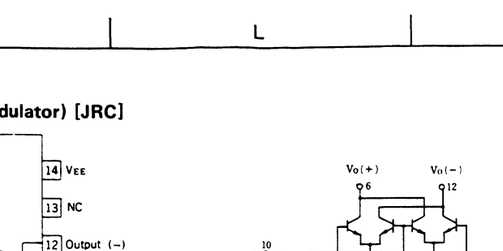

## * TC40H002 (Quad 2-Input not Gage) [TOSHIBA]




## *TC4051 (Single 8-Channel Multiplexer/Demultiplexer) [TOSHIBA]




**Block Diagram**

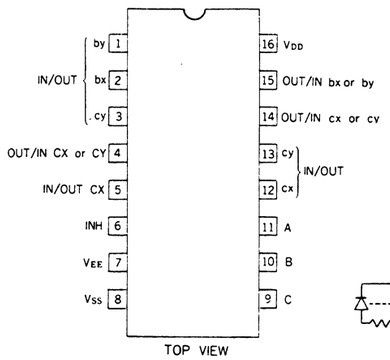



**TRUTH TABLE**

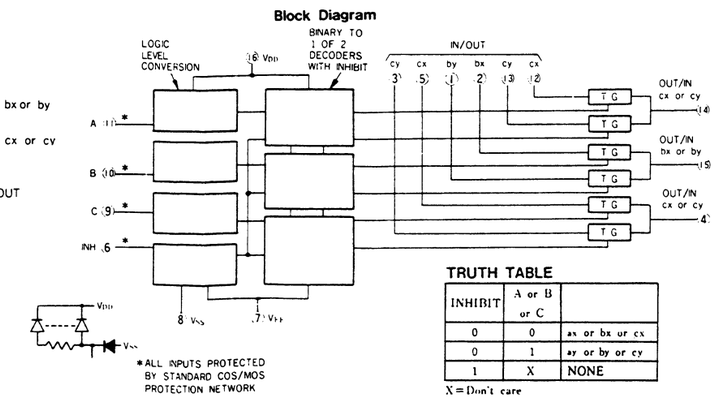
| INPUT STATES | | | "ON" CHANNEL(S) |
|---|---|---|---|
| INHIBIT | C | B | A | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | X | X | X | NONE |

X = Don't care

## *TC4053 (Triple-2 Channel Multiplexer/Demultiplexer) [TOSHIBA]




**Block Diagram**

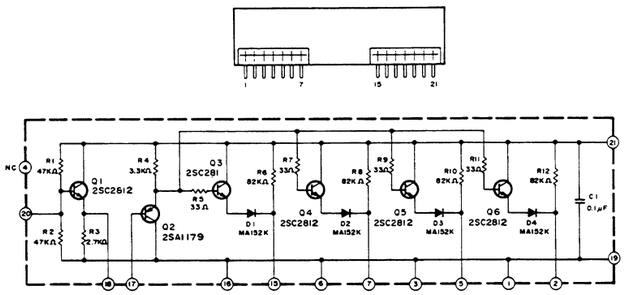

LOGIC LEVEL CONVERSION
BINARY TO 1 OF 2 DECODERS WITH INHIBIT
IN/OUT
OUT/IN cx or cy
OUT/IN bx or by
OUT/IN cx or cy
TG
*ALL INPUTS PROTECTED BY STANDARD COS/MOS PROTECTION NETWORK

**TRUTH TABLE**

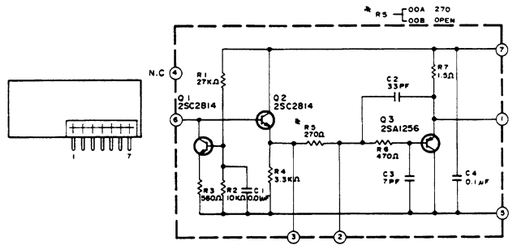
| INHIBIT | A or B or C | |
|---|---|---|
| 0 | 0 | ax or bx or cx |
| 0 | 1 | ay or by or cy |
| 1 | X | NONE |

X = Don't care

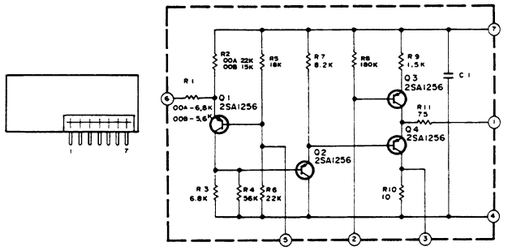
## *CBMC4070-00A [JVC]



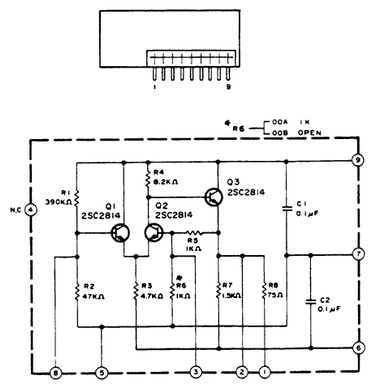

## *CBMC4073-00A -00B [JVC]



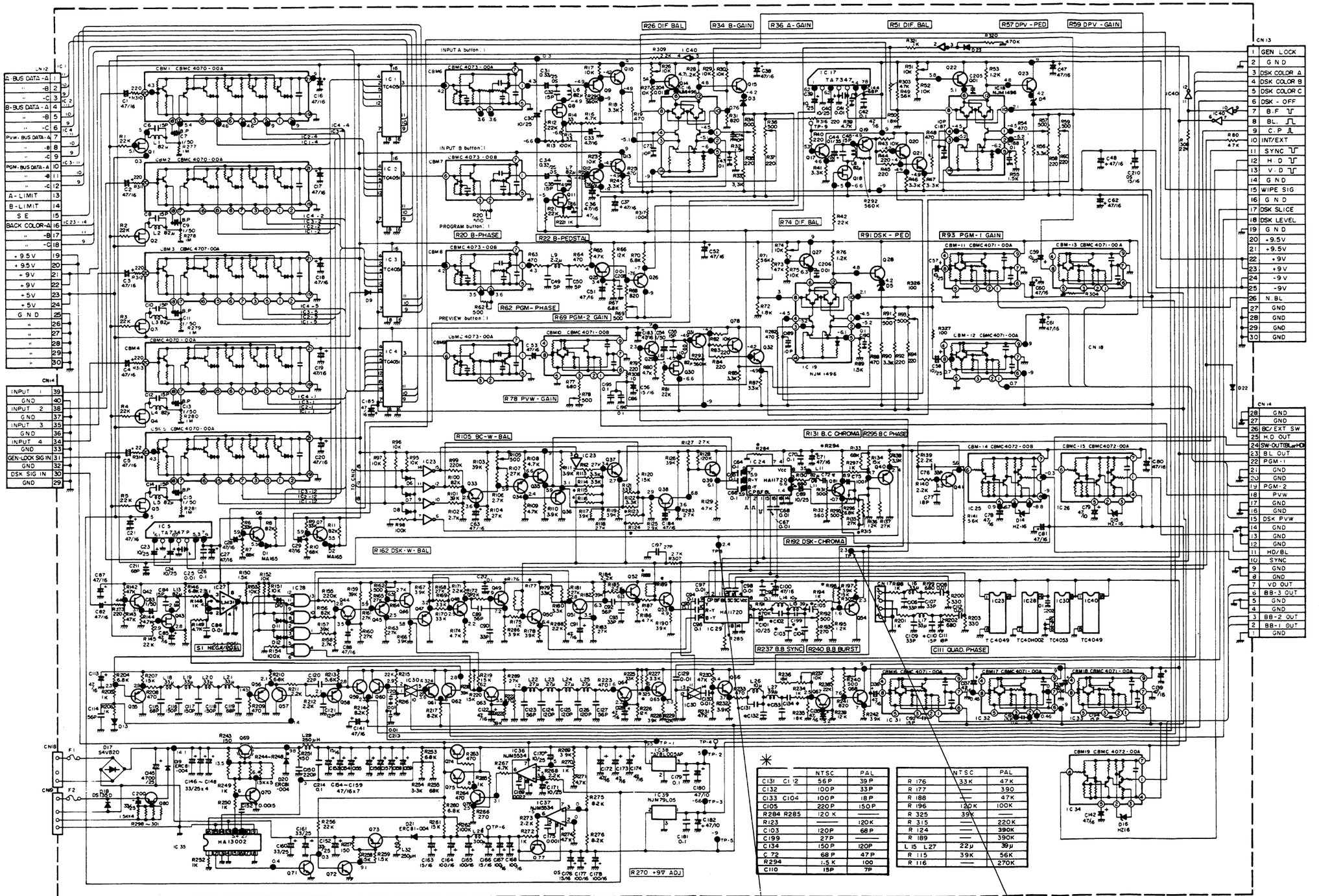

## *CBMC4072-00A -00B [JVC]




## *CBMC4071-00A -00B [JVC]



## 5.4 MA SCHEMATIC DIAGRAM




S1 Added from #1505**** and after.

"Revised on June 1989"

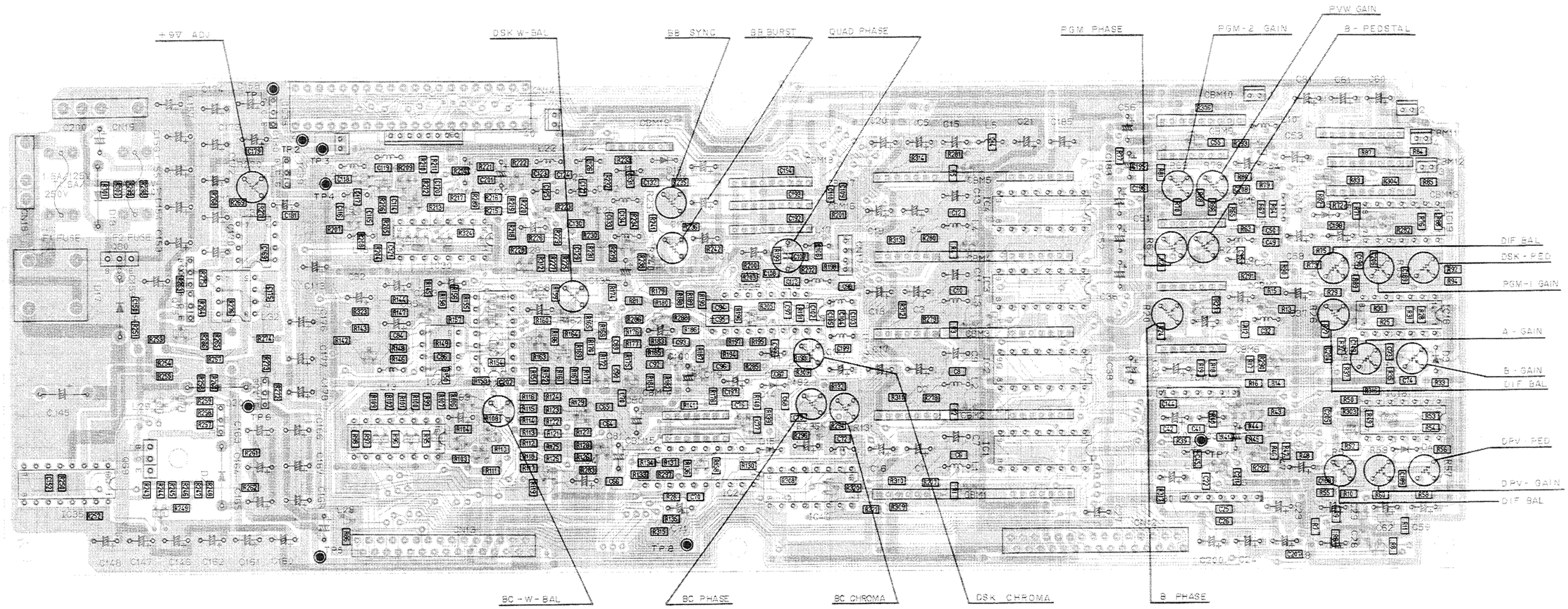
| * | NTSC | PAL |
|---|---|---|
| C131 C112 | 56P | 39P |
| C132 | 100P | 33P |
| C133 C104 | 100P | 18P |
| C105 | 220P | 150P |
| R284 R285 | 120 K | —— |
| R123 | —— | 120K |
| C103 | 120P | 68P |
| C199 | 27P | —— |
| C134 | 150P | 120P |
| C 72 | 68P | 47P |
| R294 | 1.5K | 100 |
| C110 | 15P | 7P |

| | NTSC | PAL |
|---|---|---|
| R 176 | 33K | 47K |
| R 177 | —— | 390 |
| R 188 | —— | 47K |
| R 196 | 120K | 100K |
| R 325 | 39K | —— |
| R 315 | —— | 220K |
| R 124 | —— | 390K |
| R 189 | —— | 390K |
| L 15 L27 | 22μ | 39μ |
| R 115 | 39K | 56K |
| R 116 | —— | 270K |

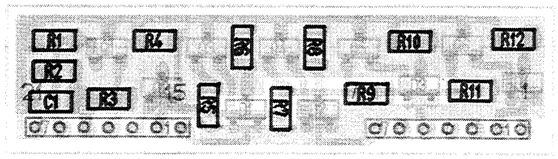


5-3 MA SCHEMATIC & BOARD (SW/LO BLOCK)

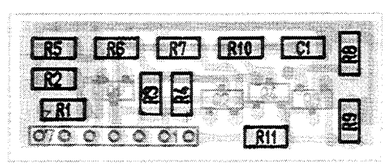
## 5.5 MA CIRCUIT BOARD



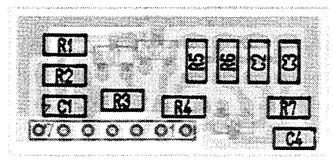

– CP CBM BOARD –



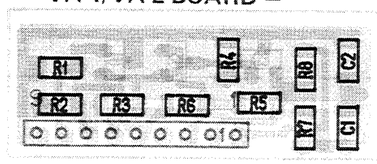

– PA-1/PA-2 BOARD –




– BA-1/BA-2 BOARD –



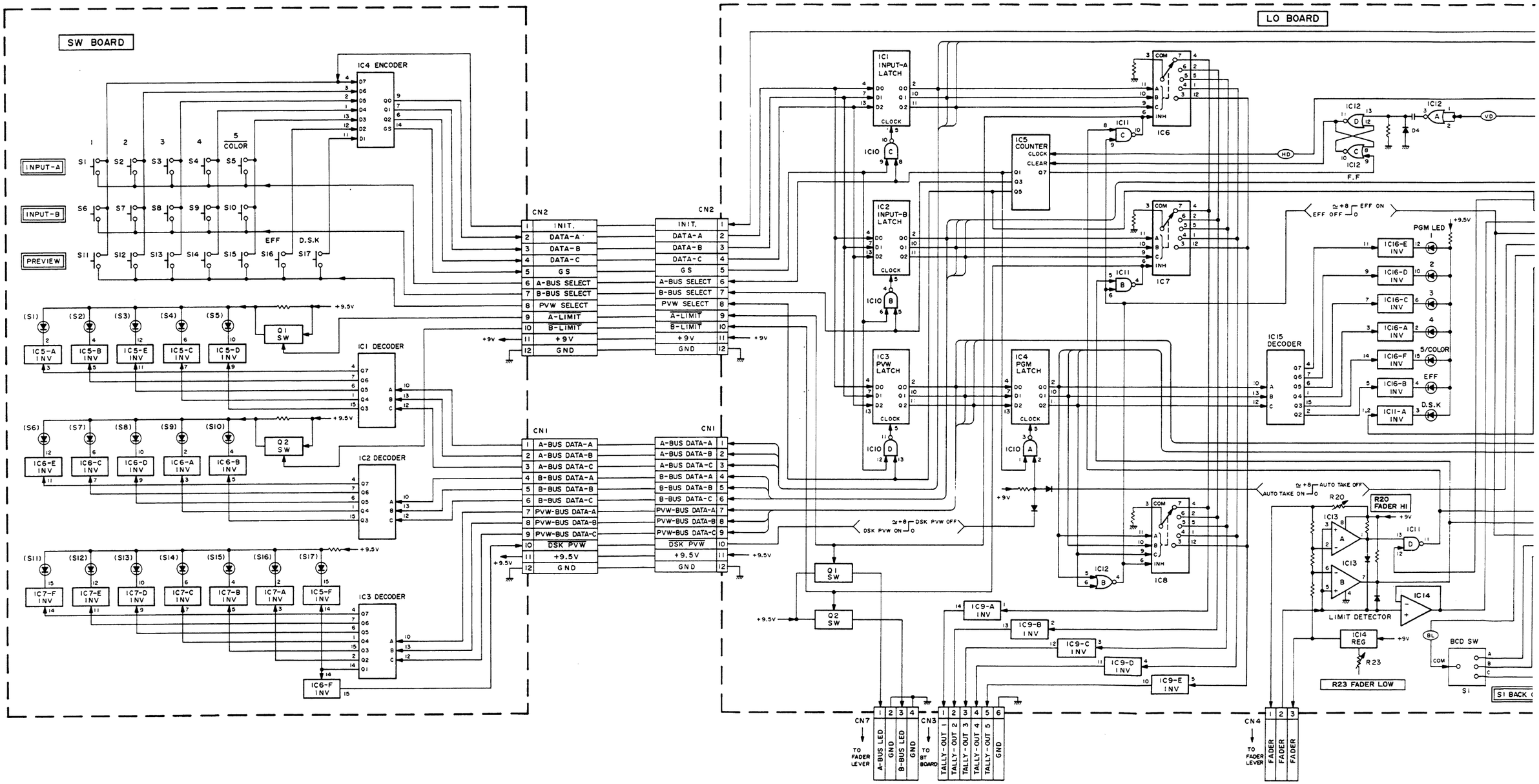

– VA-1/VA-2 BOARD –





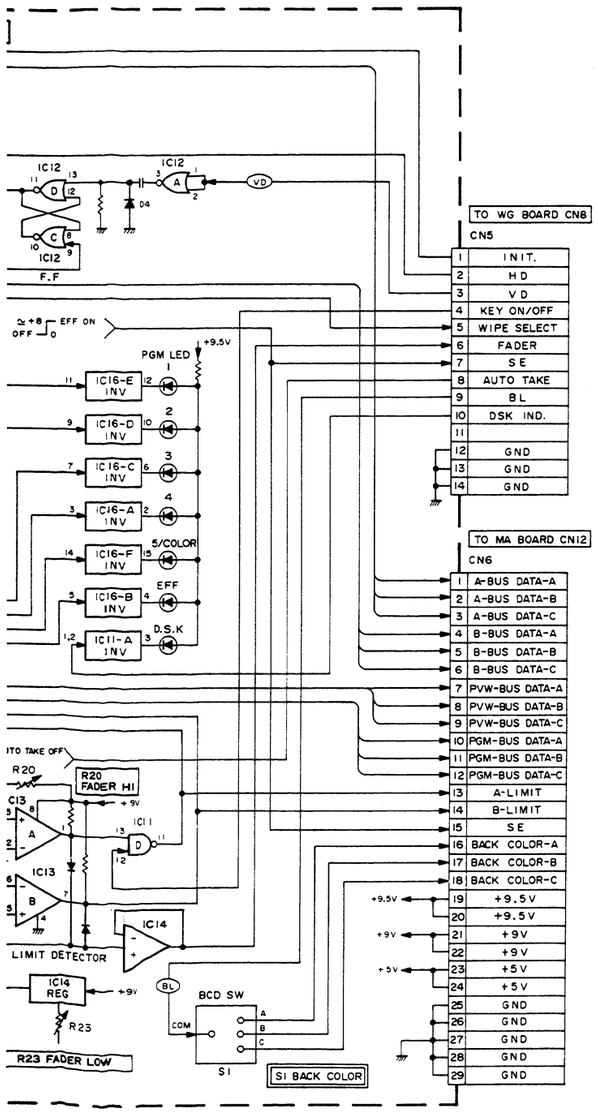

5-3 MA SCHEMATIC & BOARD (SW/LO BLOCK)

## 5.6 SW/LO BLOCK DIAGRAM

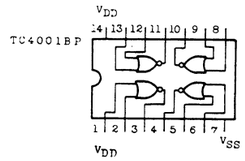




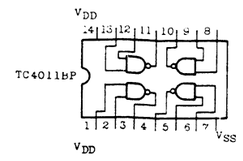

5-4 SW/LO BLOCK (MA SCHEMATIC & BOARD)



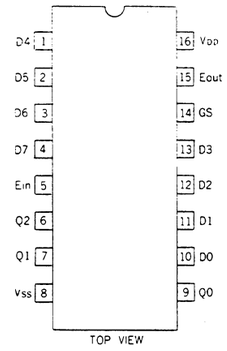

## *TC4001 (Quad Positive NOR Gate) [TOSHIBA]



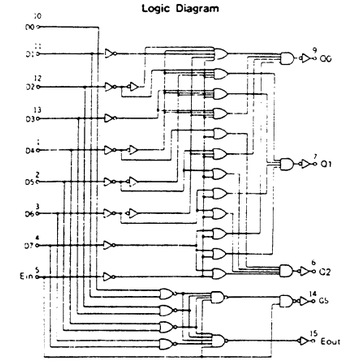

## *TC4011 (QUAD Positive NAND Gate) [TOSHIBA]




## *TC4532 (8-Bit Priority Encorder) [TOSHIBA]




Logic Diagram

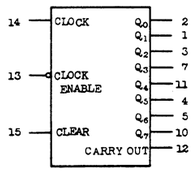



TRUTH TABLE

| INPUT | | | | | | | | | OUTPUT | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ein | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | GS | Q2 | Q1 | Q0 | EOUT |
| 0 | × | × | × | × | × | × | × | × | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | × | × | × | × | × | × | × | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | × | × | × | × | × | × | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | × | × | × | × | × | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | × | × | × | × | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | × | × | × | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | × | × | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | × | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

X = Don't Care

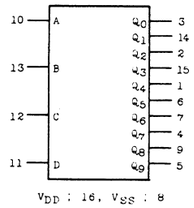
## *TC4022 (Counter) [TOSHIBA]




| INPUTS | | | SELECTED |
|---|---|---|---|
| CLOCK △ | $\overline{CE}$ △ | CLEAR | OUTPUT |
| ※ | ※ | H | $Q_0$ |
| ※ | H | L | $Q_n$ (NC) |
| L | ※ | L | $Q_n$ (NC) |
| ⌐ | L | L | $Q_n+1$ |
| ⌐ | L | L | $Q_n$ (NC) |
| H | ⌐ | L | $Q_n$ (NC) |
| H | ⌐ | L | $Q_n+1$ |

△ ; Level Change
※ ; Don't Care
NC ; No Change
CARRY OUT { "H"…$Q_0 \sim Q_3$ = "H"; "L"…$Q_4 \sim Q_7$ = "H" }

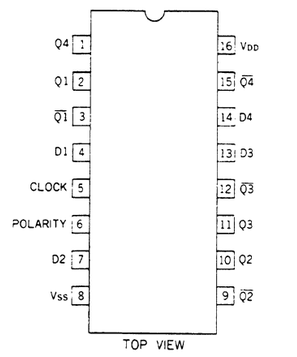
## *TC4028 (Decoder) [TOSHIBA]



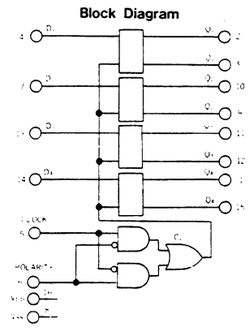

| INPUTS | | | | SELECTED OUTPUT |
|---|---|---|---|---|
| D | C | B | A | "H" |
| L | L | L | L | $Q_0$ |
| L | L | L | H | $Q_1$ |
| L | L | H | L | $Q_2$ |
| L | L | H | H | $Q_3$ |
| L | H | L | L | $Q_4$ |
| L | H | L | H | $Q_5$ |
| L | H | H | L | $Q_6$ |
| L | H | H | H | $Q_7$ |
| H | ※ | ※ | L | $Q_8$ |
| H | ※ | ※ | H | $Q_9$ |

※ Don't care

## *TC4042 (Quadruple Clock "D" Latch) [TOSHIBA]



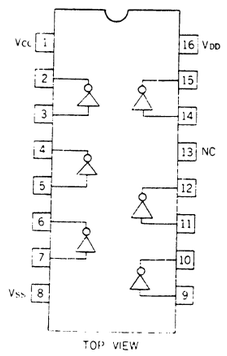

Block Diagram



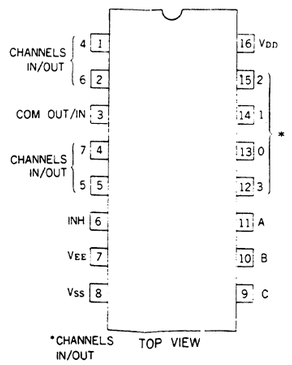
TRUTH TABLE

| CLOCK | POLARITY | Q |
|---|---|---|
| 0 | 0 | D |
| ⌐ | 0 | LATCH |
| 1 | 1 | D |
| ⌐ | 1 | LATCH |

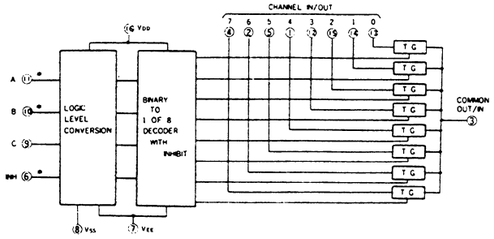
## *TC4049 (Hex Buffer/Inverter) [TOSHIBA]




## *TC4051 (Single 8-Channel Multiplexer/Demultiplexer) [TOSHIBA]




Block Diagram

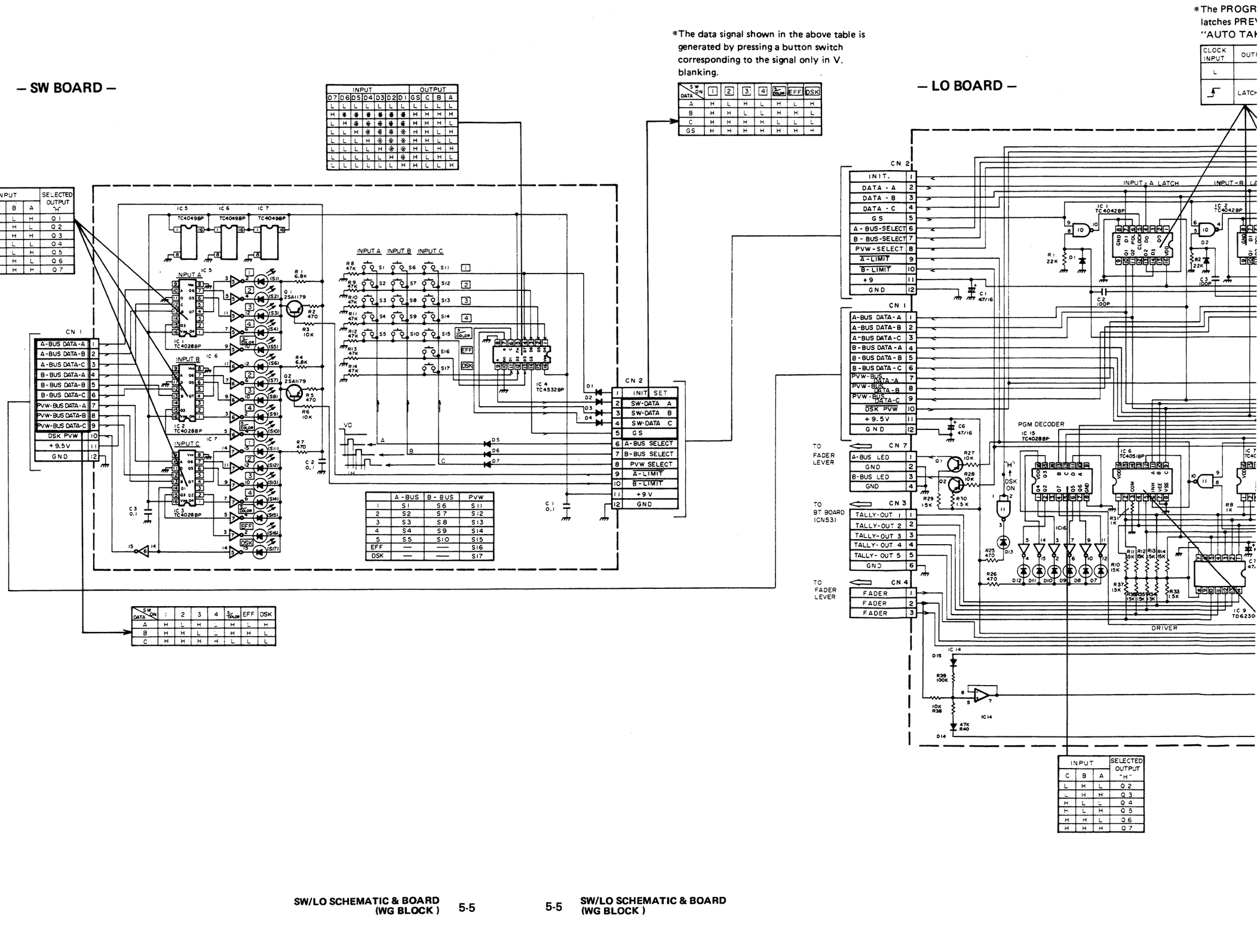



TRUTH TABLE

| INPUT STATES | | | | "ON" CHANNEL(S) |
|---|---|---|---|---|
| INHIBIT | C | B | A | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | X | X | X | NONE |

X = Don't care

## 5.7 SW/LO SCHEMATIC DIAGRAM




| SW DATA \ ON | 1 | 2 | 3 | 4 | 3 COLOR | EFF | DSK |
|---|---|---|---|---|---|---|---|
| A | H | L | H | L | H | L | H |
| B | H | H | L | L | H | H | L |
| C | H | H | H | H | L | L | L |
| GS | H | H | H | H | H | H | H |

| INPUT | | | | | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | GS | C | B | A | |
| L | L | L | L | L | L | L | L | L | L | L | |
| H | * | * | * | * | * | * | H | H | H | H | |
| L | H | * | * | * | * | * | H | H | H | L | |
| L | L | H | * | * | * | * | H | H | L | H | |
| L | L | L | H | * | * | * | H | H | L | L | |
| L | L | L | L | H | * | * | H | L | H | H | |
| L | L | L | L | L | H | * | H | L | H | L | |
| L | L | L | L | L | L | H | H | L | L | H | |

| INPUT | | | | SELECTED OUTPUT "H" |
|---|---|---|---|---|
| C | B | A | | |
| L | L | L | H | Q 1 |
| L | L | H | L | Q 2 |
| L | L | H | H | Q 3 |
| L | H | L | L | Q 4 |
| L | H | L | H | Q 5 |
| L | H | H | L | Q 6 |
| L | H | H | H | Q 7 |

| | A-BUS | B-BUS | PVW |
|---|---|---|---|
| 1 | S1 | S6 | S11 |
| 2 | S2 | S7 | S12 |
| 3 | S3 | S8 | S13 |
| 4 | S4 | S9 | S14 |
| 5 | S5 | S10 | S15 |
| EFF | — | — | S16 |
| DSK | — | — | S17 |

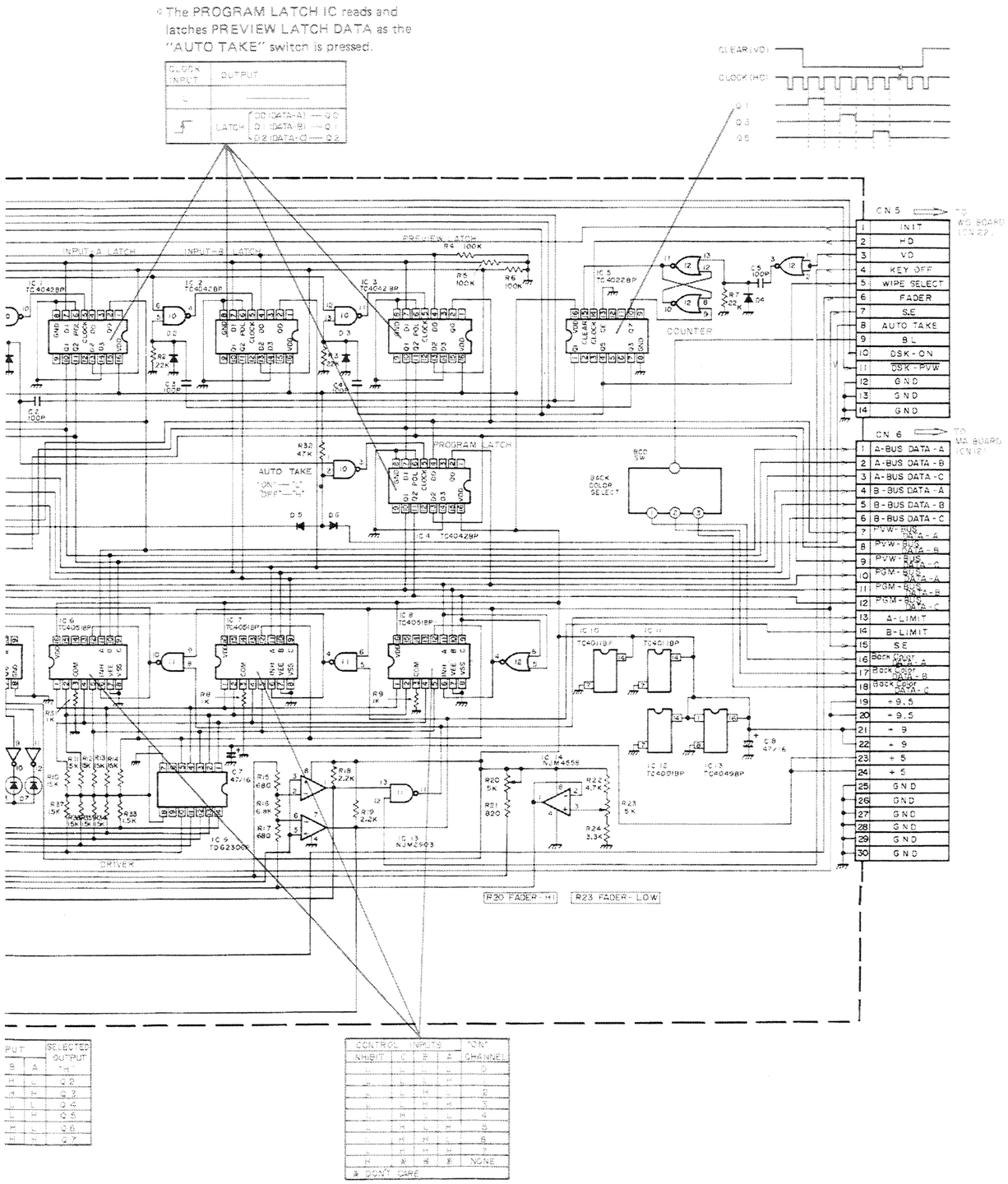
| CLOCK INPUT | OUT |
|---|---|
| L | |
| ⌐ | LATCH |

| INPUT | | | SELECTED OUTPUT "H" |
|---|---|---|---|
| C | B | A | |
| L | H | L | Q 2 |
| L | H | H | Q 3 |
| H | L | L | Q 4 |
| H | L | H | Q 5 |
| H | H | L | Q 6 |
| H | H | H | Q 7 |



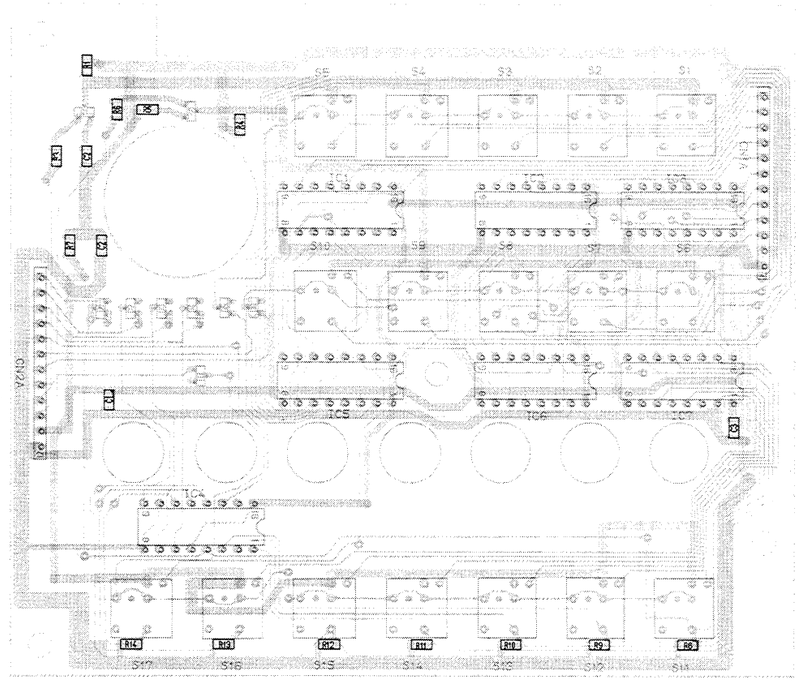
5-5 SW/LO SCHEMATIC & BOARD (WG BLOCK)

## 5.8 WG/LO CIRCUIT BOARD

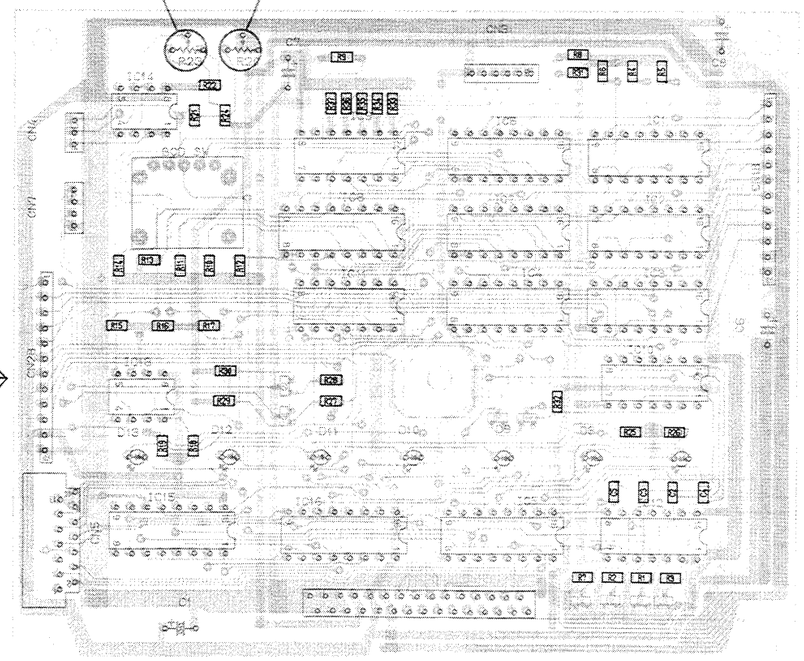





— SW BOARD —

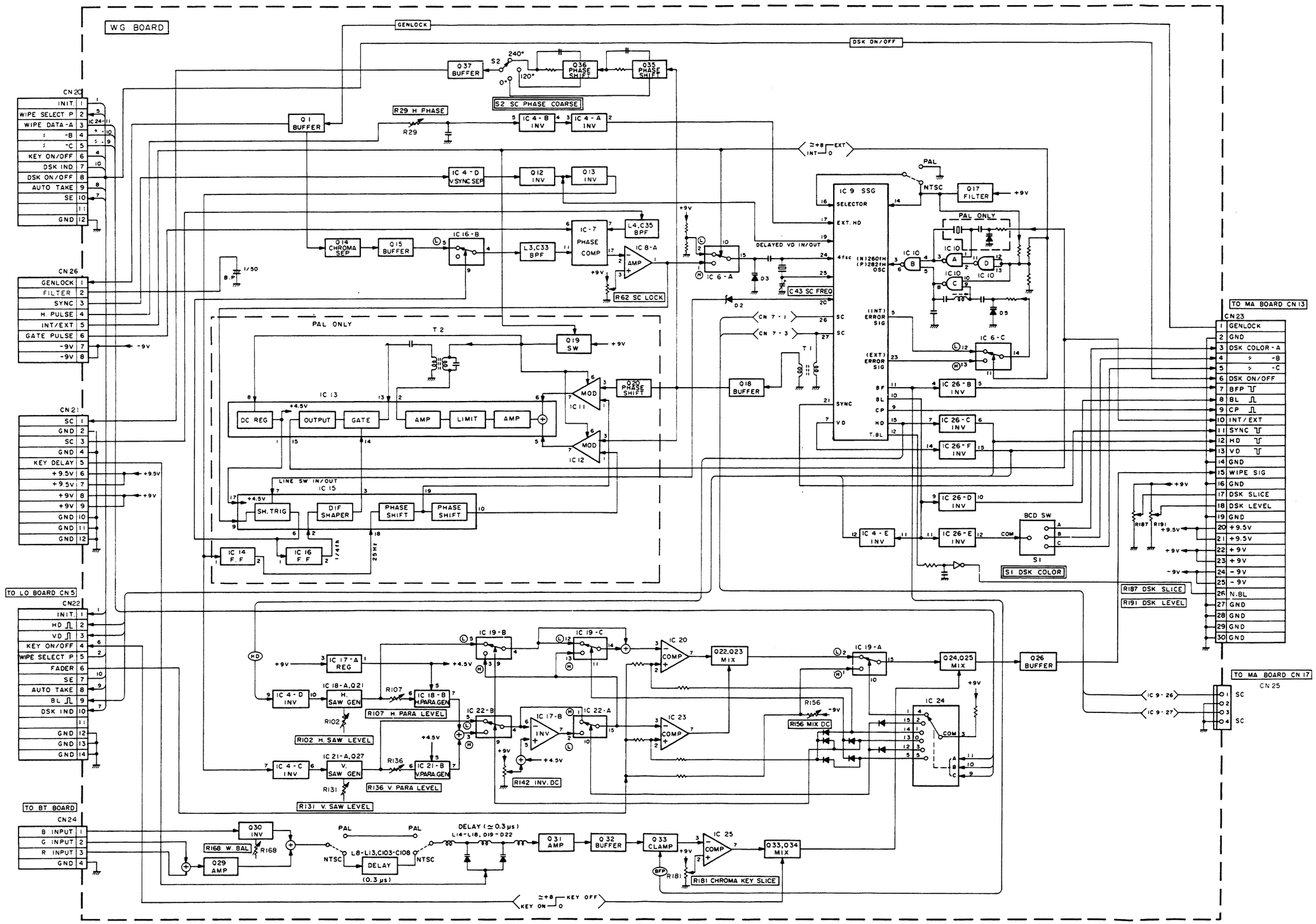


— LO BOARD —

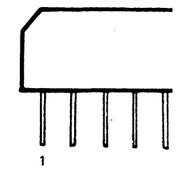



5-5 SW/LO SCHEMATIC & BOARD (WG BLOCK)

## 5.9 WG BLOCK DIAGRAM

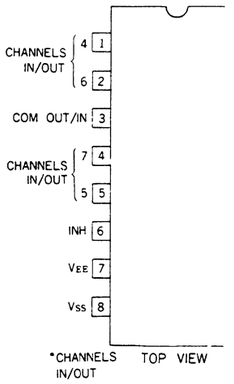



***AN612**



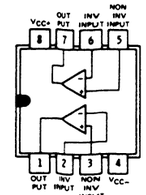

***NJM311**

***TC4051**




***TL062**

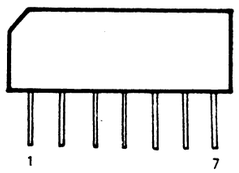
**TL062, TL062A, TL**
**JG OR P DUAL-IN-L**
**(PACKAGE (TOP VI**

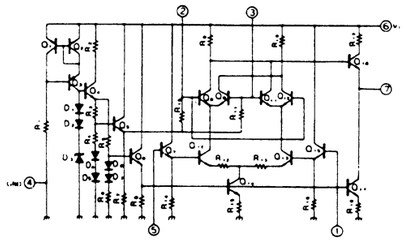



WG BLOCK (SW/LO SCHEMATIC & BOARD) 5-6

5-6 WG BLOCK (SW/LO SCHEMATIC & BOARD)

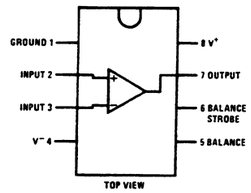
## *AN612



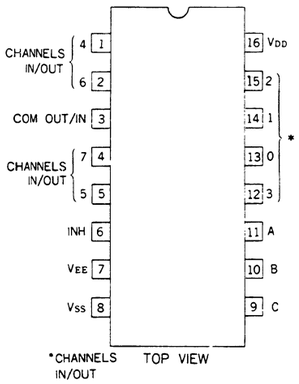



## *NJM311

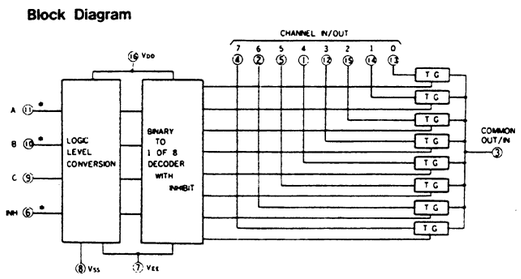
Dual-In-Line Package




## *TC4051




**Block Diagram**



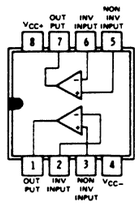

**TRUTH TABLE**

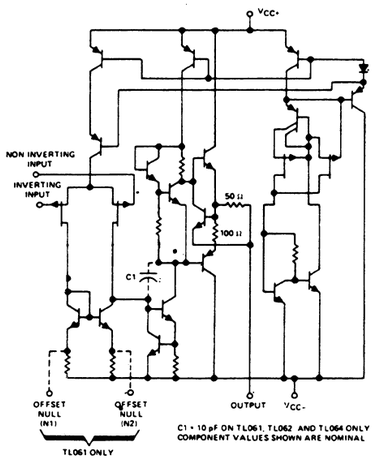
| INPUT STATES | | | | "ON" CHANNEL(S) |
|---|---|---|---|---|
| INHIBIT | C | B | A | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | X | X | X | NONE |

X = Don't care

## *TL062

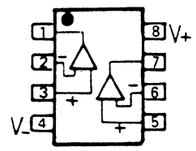
**TL062, TL062A, TL062B JG OR P DUAL-IN-LINE (PACKAGE (TOP VIEW)**

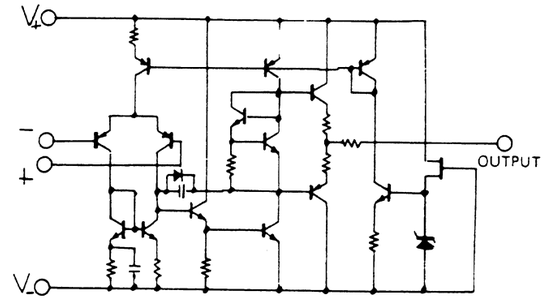




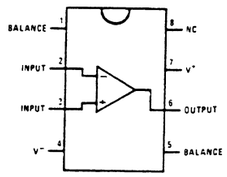

## *NJM4558



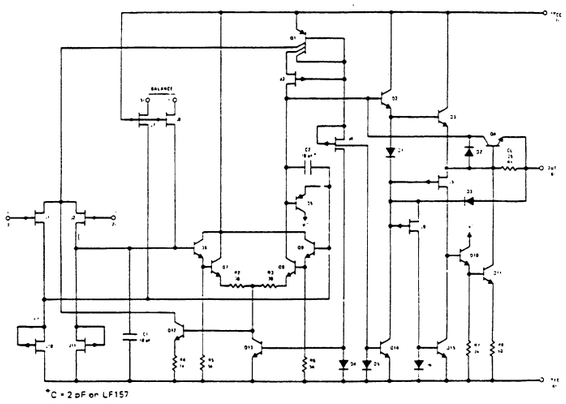




## *LF356
## 357

Dual-In-Line Package (N)

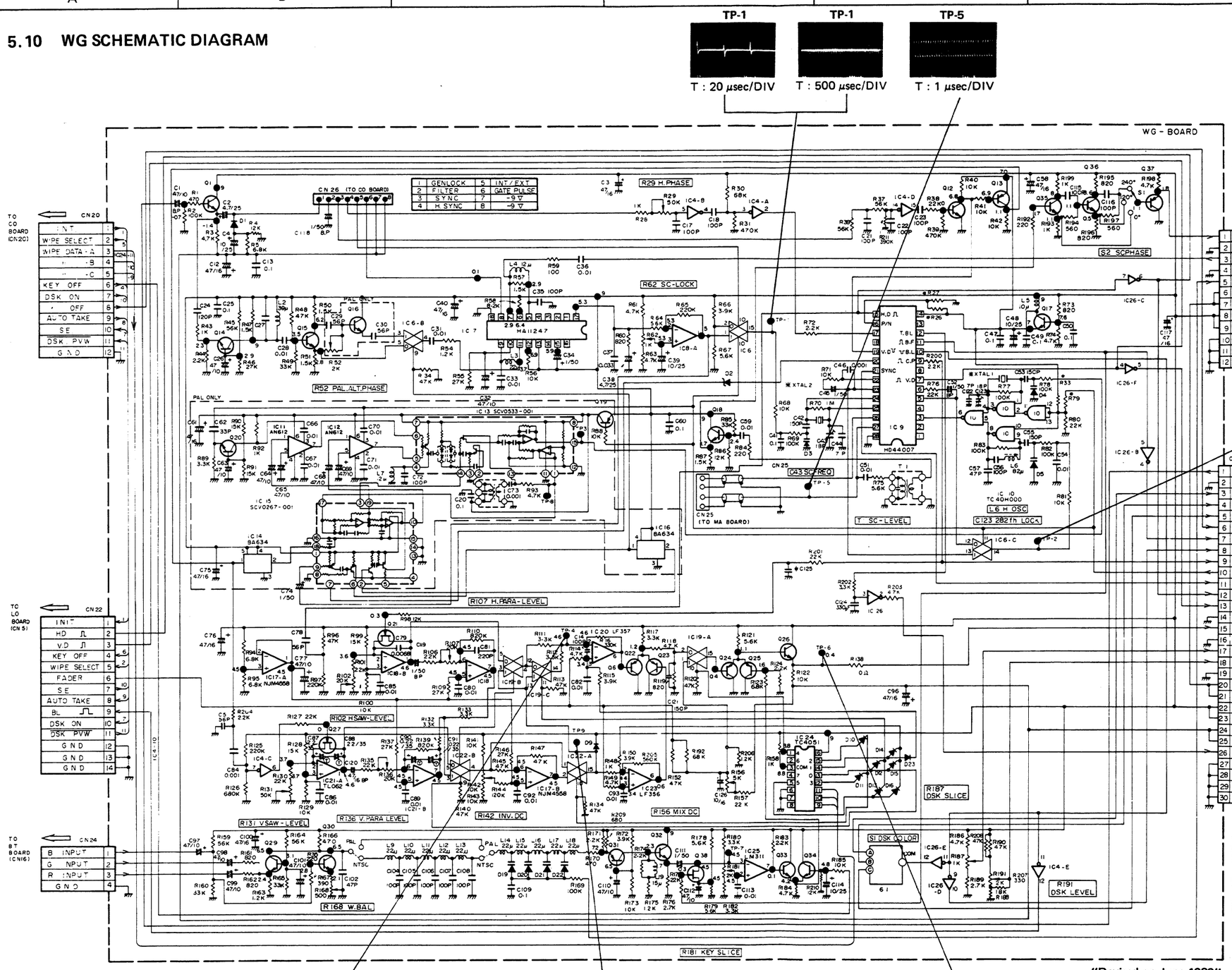



Order Number LF355N, LF356N or LF357N
See NS Package N08B



## 5.10 WG SCHEMATIC DIAGRAM

## 5.11 WG CIRCUIT BOARD




WIPE CODE

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| IC 11-9 | A | 0 | 1 | 0 | 1 | 0 | 1 | | |
| IC 11-10 | B | 0 | 0 | 1 | 1 | 0 | 0 | | 1 |
| IC 11-11 | C | 0 | 0 | 0 | 0 | 1 | 1 | | 1 |

*

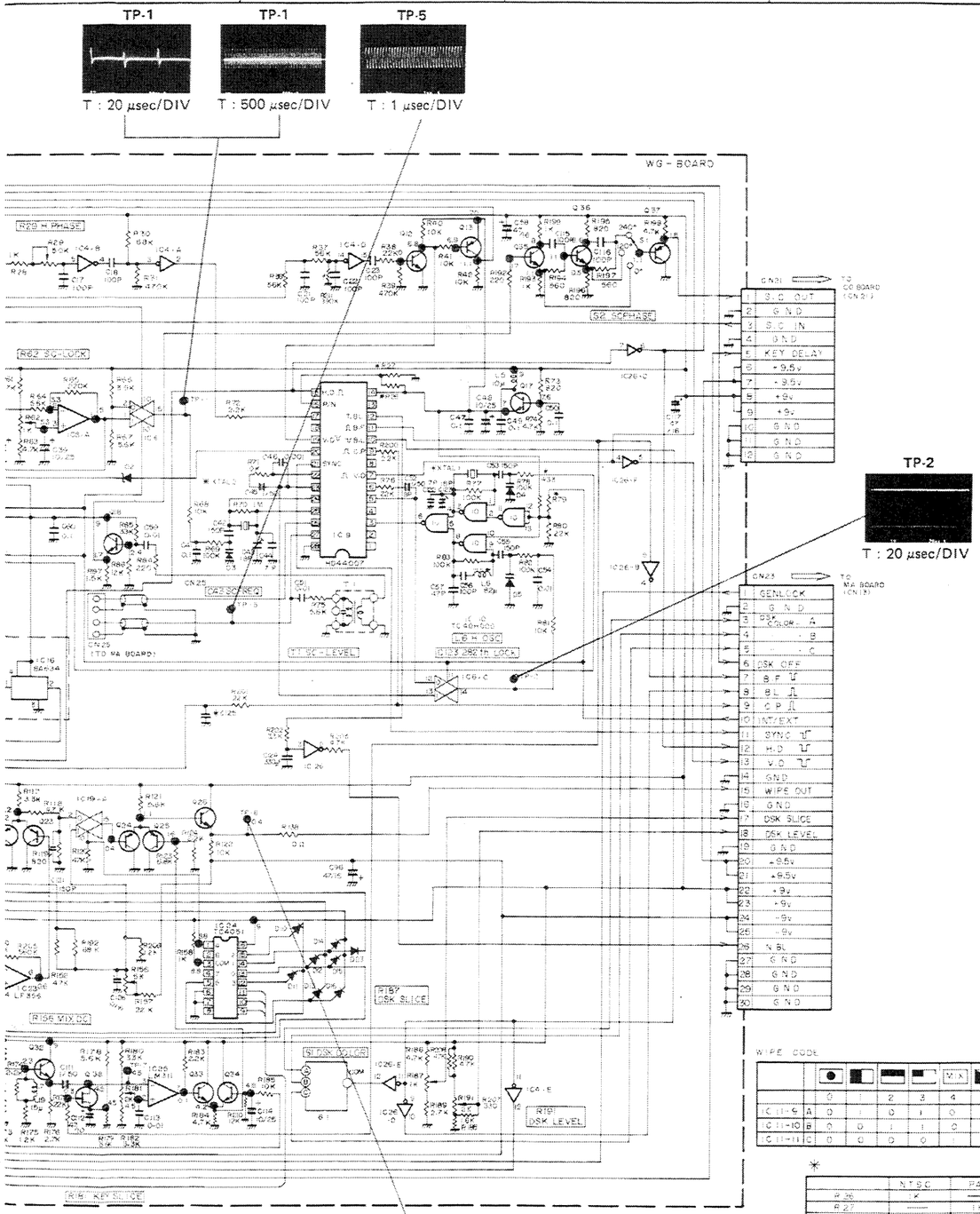
| | NTSC | PAL |
|---|---|---|
| R 26 | 1K | — |
| R 27 | — | 1K |
| R 33 | 47K | — |
| R 79 | — | 47K |
| C125 | — | 15P |
| C 27 | 47P | 33P |
| XTAL 1 | — | SCV0349-001 |
| XTAL 2 | SCV0347-001 | SCV0348-001 |
| T 1 | GC44286-001 | SCV0171-001 |
| T 2 | — | SCV0171-001 |

— : OPEN

WG SCHEMATIC & BOARD (CO BLOCK) 5-7

5-7 WG SCHEMATIC & BOARD (CO BLOCK)

## 5.11 WG CIRCUIT BOARD

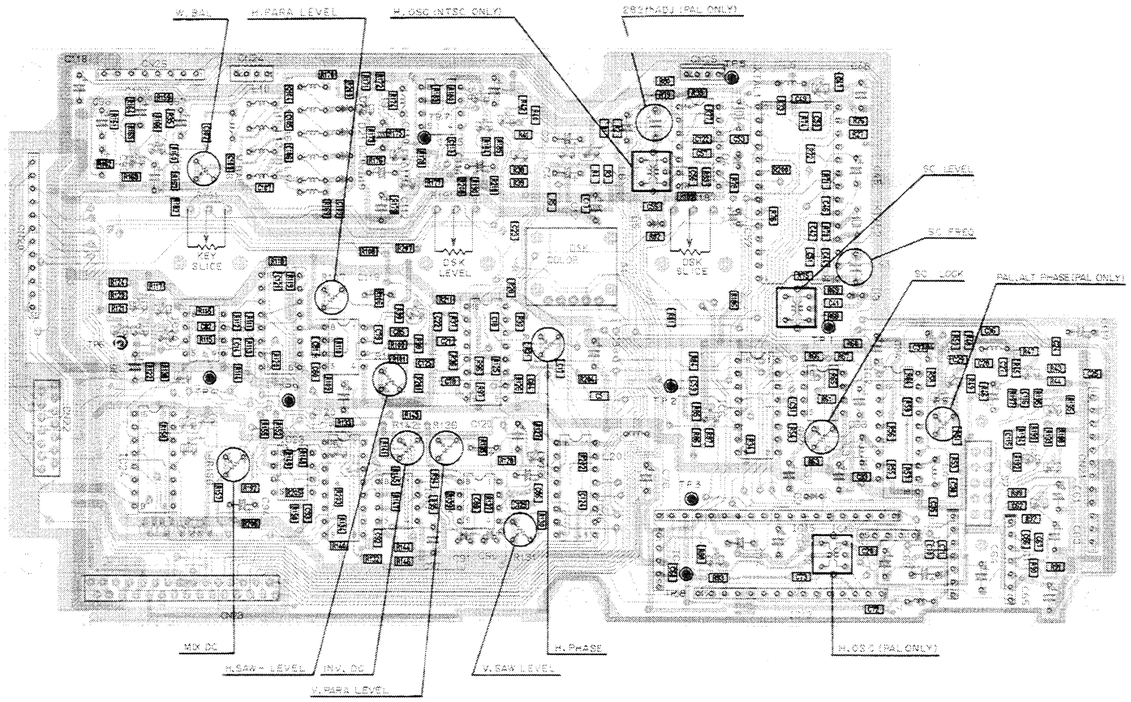



| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|---|
| C11-9 | A | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| C11-10 | B | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| C11-11 | C | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

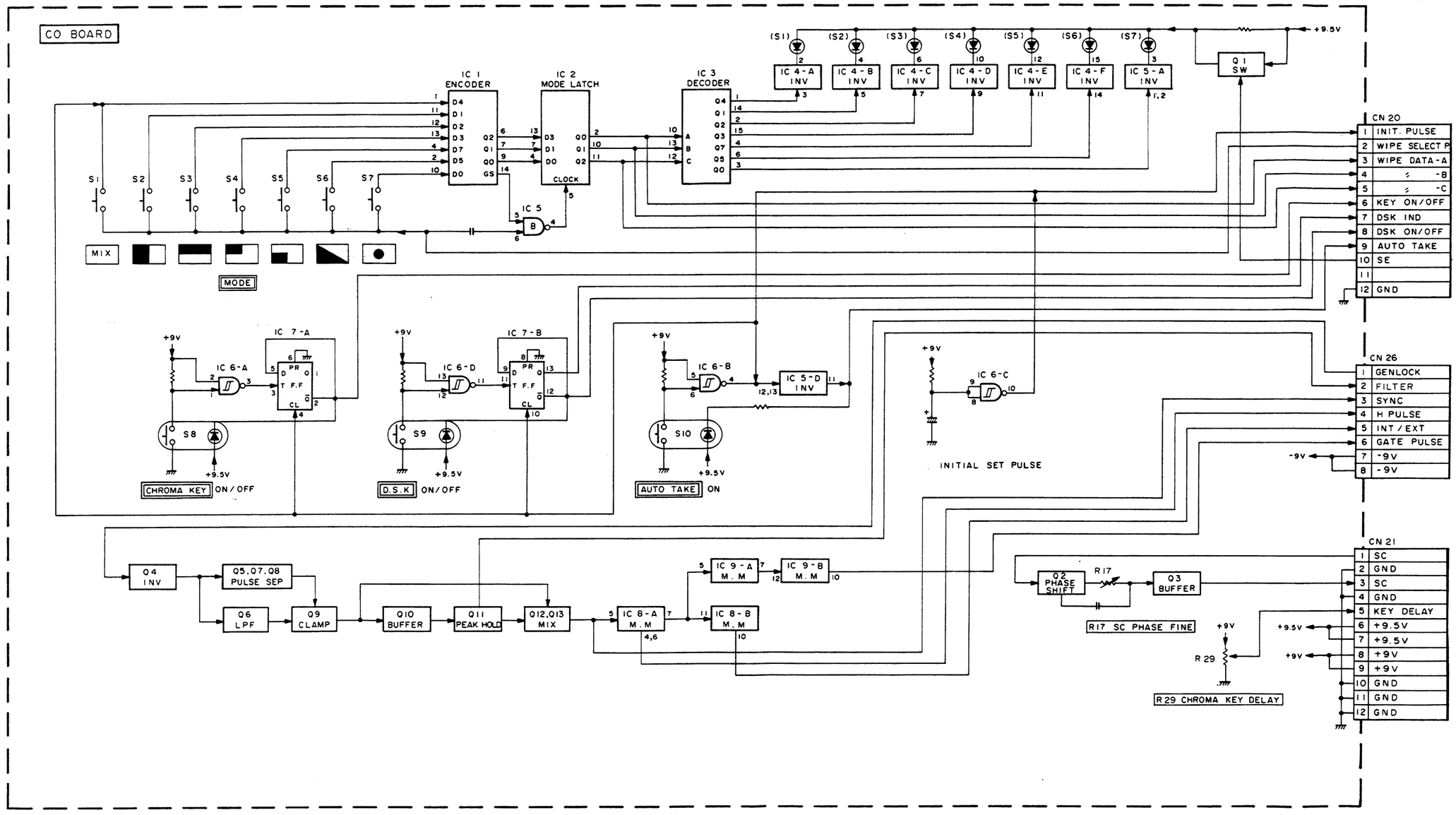
WIPE CODE

| | NTSC | PAL |
|---|---|---|
| R26 | 2K | —— |
| R27 | —— | 1K |
| R33 | 47K | —— |
| R79 | —— | 47K |
| C105 | —— | 15P |
| C27 | 47P | 33P |
| X'TAL1 | —— | SCV0349-00 |
| X'TAL2 | SCV0347-001 | SCV0348-00 |
| T2 | GC44286-001 | SCV0171-001 |
| T3 | —— | SCV0171-001 |

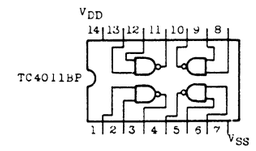
—— : OPEN



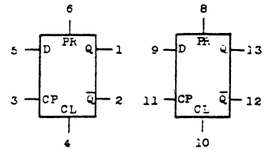
## 5.12 CO BLOCK DIAGRAM




### *TC4011 (Quad Positive NAND Gate) [TOSHIBA]




### *TC4013 (Dual Flip Flop) [TOSHIBA]

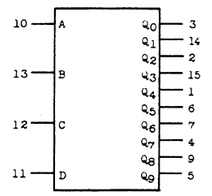



$V_{DD}$ ; 14, $V_{SS}$ ; 7

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| CL | PR | D | CP △ | $Q_{n+1}$ | $\bar{Q}_{n+1}$ |
| L | H | ※ | ※ | H | L |
| H | L | ※ | ※ | L | H |
| H | H | ※ | ※ | L | H |
| L | L | L | ↓ | L | H |
| L | L | H | ↓ | H | L |
| L | L | ※ | ↑ | $Q_n$ • | $\bar{Q}_n$ • |

※ ; Don't Care
△ ; Level Change
• ; No Change

### *TC4028 (Decorder) [TOSHIBA]

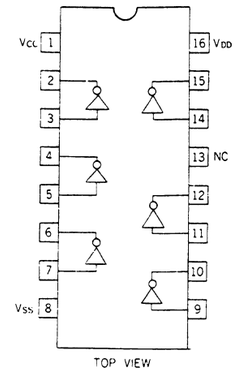



$V_{DD}$ : 16, $V_{SS}$ : 8

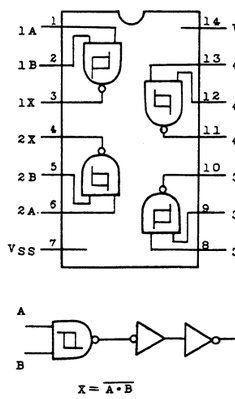
| INPUTS | | | | SELECTED OUTPUT "H" |
|---|---|---|---|---|
| D | C | B | A | |
| L | L | L | L | $Q_0$ |
| L | L | L | H | $Q_1$ |
| L | L | H | L | $Q_2$ |
| L | L | H | H | $Q_3$ |
| L | H | L | L | $Q_4$ |
| L | H | L | H | $Q_5$ |
| L | H | H | L | $Q_6$ |
| L | H | H | H | $Q_7$ |
| H | ※ | ※ | L | $Q_8$ |
| H | ※ | ※ | H | $Q_9$ |

※ Don't care

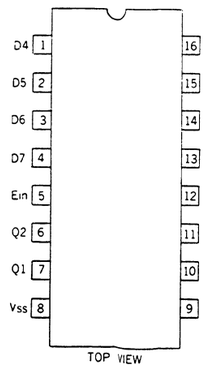
### *TC4049 (Hex Buffer/Inverte [TOSHIBA]

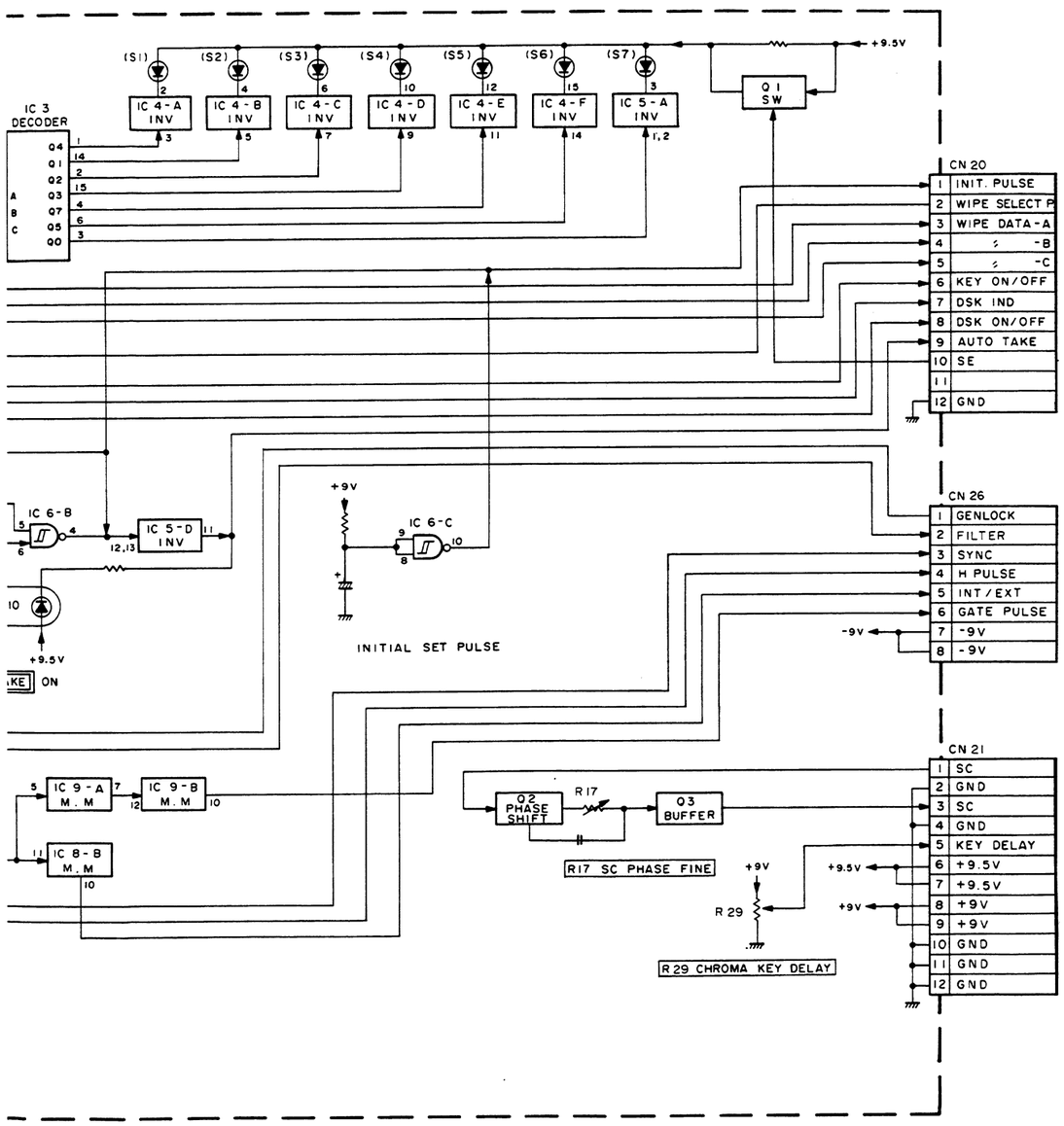



### *TC4093 (NAND Schmitt Tri [TOSHIBA]

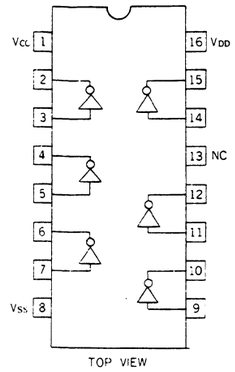



### *TC4532 (8-Bit Priority

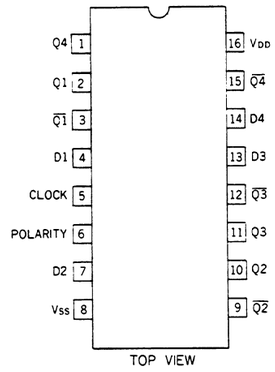




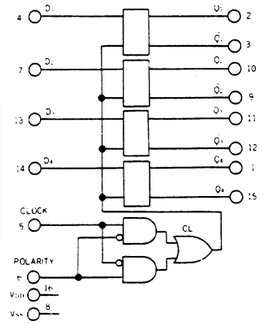

***TC4049 (Hex Buffer/Inverter) [TOSHIBA]**



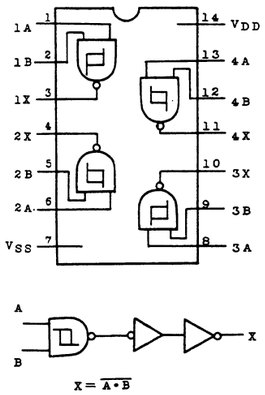

***TC4042 (Quadruple Clock "D" Latch) [TOSHIBA]**



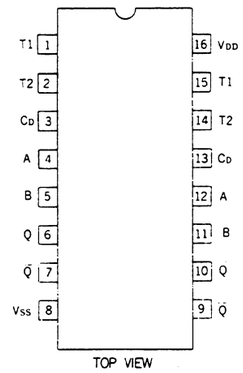

| CLOCK | POLARITY | Q |
|---|---|---|
| 0 | 0 | D |
| ↑ | 0 | LATCH |
| 1 | 1 | D |
| ↓ | 1 | LATCH |

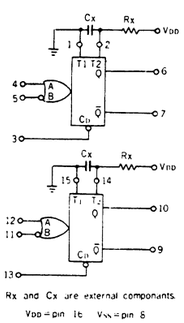


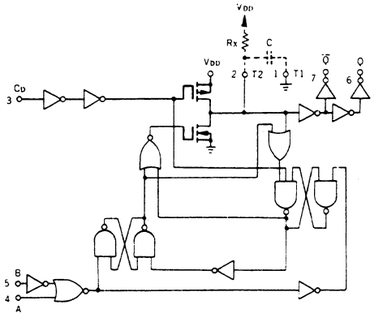

***TC4093 (NAND Schmitt Trig.) [TOSHIBA]**



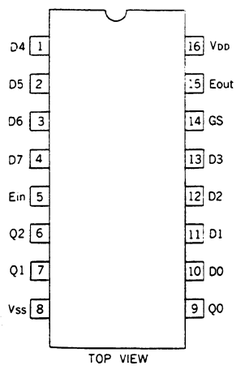

***TC4538**



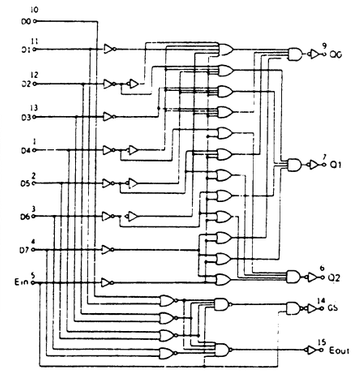

***TC4532 (8-Bit Priority Encorder)) [TOSHIBA]**



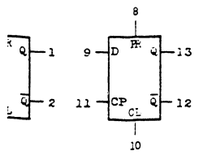

**TRUTH TABLE**

| INPUT | | | | | | | | | | OUTPUT | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ein | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | GS | Q2 | Q1 | Q0 | Eout |
| 0 | × | × | × | × | × | × | × | × | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | × | × | × | × | × | × | × | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | × | × | × | × | × | × | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | × | × | × | × | × | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | × | × | × | × | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | × | × | × | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | × | × | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | × | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

X = Don't Care



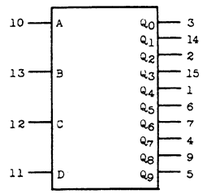

**:4013 (Dual Flip Flop) [TOSHIBA]**




| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| CL | PR | D | CP △ | $Q_{n+1}$ | $\bar{Q}_{n+1}$ |
| L | H | ※ | ※ | H | L |
| H | L | ※ | ※ | L | H |
| H | H | ※ | ※ | L | H |
| L | L | L | ↓ | L | H |
| L | L | H | ↓ | H | L |
| L | L | ※ | ↑ | $Q_n$ • | $\bar{Q}_n$ • |

※ ; Don't Care
△ ; Level Change
• ; No Change

***TC4028 (Decorder) [TOSHIBA]**




| INPUTS | | | | SELECTED OUTPUT "H" |
|---|---|---|---|---|
| D | C | B | A | |
| L | L | L | L | $Q_0$ |
| L | L | L | H | $Q_1$ |
| L | L | H | L | $Q_2$ |
| L | L | H | H | $Q_3$ |
| L | H | L | L | $Q_4$ |
| L | H | L | H | $Q_5$ |
| L | H | H | L | $Q_6$ |
| L | H | H | H | $Q_7$ |
| H | ※ | ※ | L | $Q_8$ |
| H | ※ | ※ | H | $Q_9$ |

※ Don't care

## 5.13 CO SCHEMATIC DIAGRAM

| E IN | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | GS | Q2 | Q1 | Q0 | E OUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | ※ | ※ | ※ | ※ | ※ | ※ | ※ | ※ | L | L | L | L | L |
| H | L | L | L | L | L | L | L | L | L | L | L | L | H |
| H | H | ※ | ※ | ※ | ※ | ※ | ※ | ※ | H | H | H | H | L |
| H | L | H | ※ | ※ | ※ | ※ | ※ | ※ | H | H | H | L | L |
| H | L | L | H | ※ | ※ | ※ | ※ | ※ | H | H | L | H | L |
| H | L | L | L | H | ※ | ※ | ※ | ※ | H | H | L | L | L |
| H | L | L | L | L | H | ※ | ※ | ※ | H | L | H | H | L |
| H | L | L | L | L | L | H | ※ | ※ | H | L | H | L | L |
| H | L | L | L | L | L | L | H | ※ | H | L | L | H | L |
| H | L | L | L | L | L | L | L | H | H | L | L | L | L |

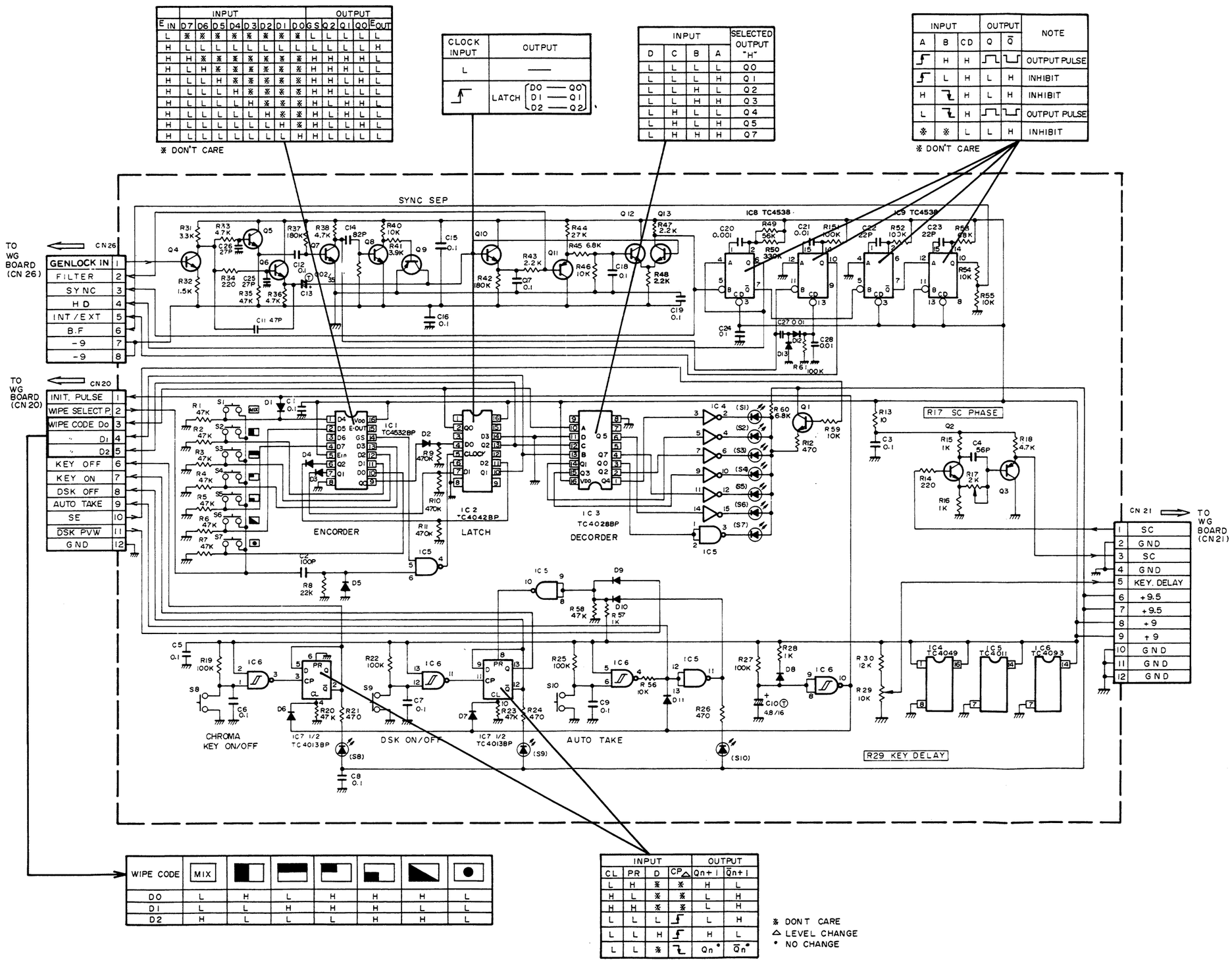
※ DON'T CARE

| CLOCK INPUT | OUTPUT |
|---|---|
| L | —— |
| ⌐ | LATCH (D0 —— Q0, D1 —— Q1, D2 —— Q2) |

| INPUT D | C | B | A | SELECTED OUTPUT "H" |
|---|---|---|---|---|
| L | L | L | L | Q0 |
| L | L | L | H | Q1 |
| L | L | H | L | Q2 |
| L | L | H | H | Q3 |
| L | H | L | L | Q4 |
| L | H | L | H | Q5 |
| L | H | H | H | Q7 |

| INPUT A | B | CD | OUTPUT Q | $\bar{Q}$ | NOTE |
|---|---|---|---|---|---|
| ⌐ | H | H | ⌐ | ⌙ | OUTPUT PULSE |
| ⌐ | L | H | L | H | INHIBIT |
| H | ⌙ | H | L | H | INHIBIT |
| L | ⌙ | H | ⌐ | ⌙ | OUTPUT PULSE |
| ※ | ※ | L | L | H | INHIBIT |

※ DON'T CARE

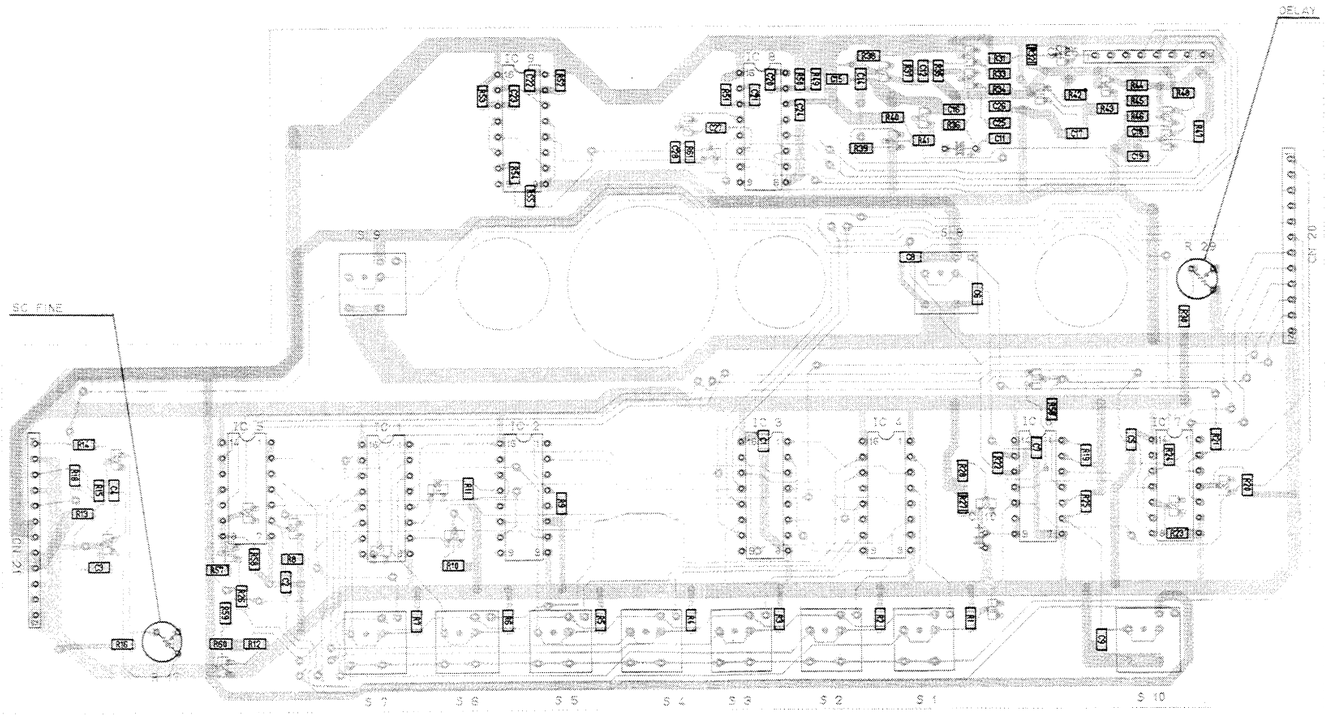



| WIPE CODE | MIX | | | | | | |
|---|---|---|---|---|---|---|---|
| D0 | L | H | L | H | H | H | L |
| D1 | L | L | H | H | H | L | L |
| D2 | H | L | L | L | H | H | L |

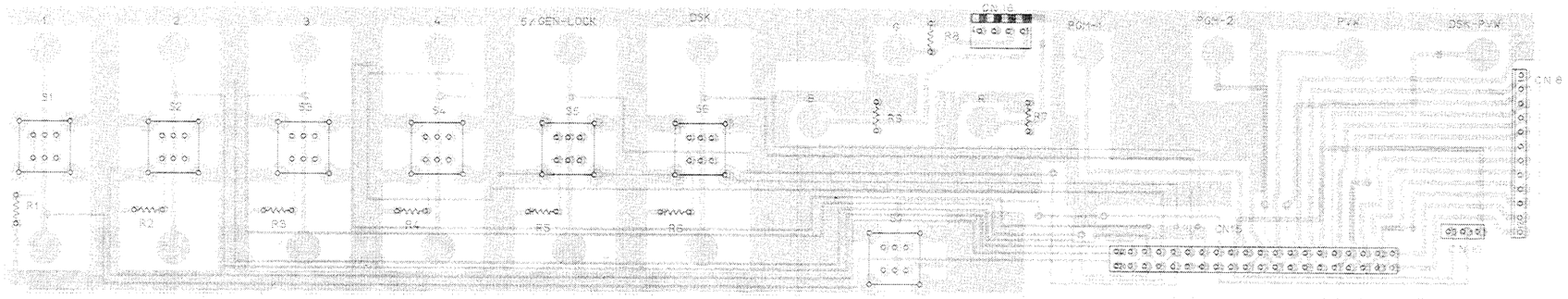
| INPUT CL | PR | D | CP △ | OUTPUT Qn+1 | $\bar{Q}$n+1 |
|---|---|---|---|---|---|
| L | H | ※ | ※ | H | L |
| H | L | ※ | ※ | L | H |
| H | H | ※ | ※ | L | H |
| L | L | L | ⌐ | L | H |
| L | L | H | ⌐ | H | L |
| L | L | ※ | ⌙ | Qn• | $\bar{Q}$n• |

※ DONT CARE
△ LEVEL CHANGE
• NO CHANGE

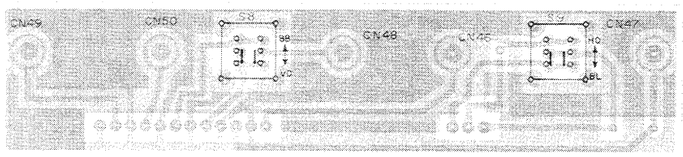
## 5.14 CO CIRCUIT BOARD



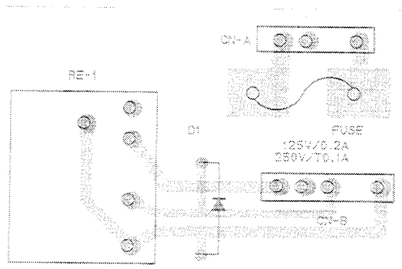
## 5.15 BT CIRCUIT BOARD

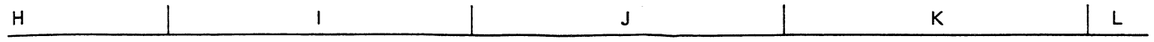



## 5.16 BC CIRCUIT BOARD




## 5.17 FU CIRCUIT BOARD






5-10 **BT, BC & FU BOARD (CO SCHEMATIC & BOARD)**

# SECTION 6
# ELECTRICAL PARTS LIST

1. IMPORTANT SAFETY NOTICE

**Parts identified by the ⚠ symbol are critical for safety. Replace with parts number specified. For maximum reliability and performance, all other replacement parts should be identical to those specified.**

2. Abbreviations in this list are as follows:

RESISTORS – All resistance values are in ohms (Ω).

| | | |
|---|---|---|
| K | : | 1 000 |
| M | : | 1 000 000 |
| CR | : | Carbon Resistor |
| Comp. R | : | Composition Resistor |
| WR | : | Wire Wound Resistor |
| OMR | : | Oxide Metal Film Resistor |
| VR | : | Variable Resistor (Potentiometer) |
| MFR | : | Metal Film Resistor |

CAPACITORS – All capacitance values are in μF, unless otherwise indicated.

| | | |
|---|---|---|
| P | : | μμF |
| C Cap | : | Ceramic Capacitor |
| E Cap | : | Electrolytic Capacitor |
| FM Cap | : | Film Mica Capacitor |
| MM Cap | : | Metalized Mylar Capacitor |
| MP Cap | : | Metalized Paper Capacitor |
| MY Cap | : | Mylar Capacitor |
| NP Cap | : | Non-polar Capacitor |
| PC Cap | : | Polycarbonate Capacitor |
| PP Cap | : | Poly Pro Capacitor |
| PS Cap | : | Polystyrol Capacitor |
| T Cap | : | Tantalum Capacitor |
| TR Cap | : | Trimmer Capacitor |

Tolerances of resistors or capacitors are as follows:

| | | |
|---|---|---|
| M | : | ± 20 % |
| K | : | ± 10 % |
| J | : | ± 5 % |
| G | : | ± 2 % |
| F | : | ± 1 % |

## 6.1 MA BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| IC 1 | TC4051BP | IC (M) | TOSHIBA |
| IC 2 | " | " | " |
| IC 3 | " | " | " |
| IC 4 | " | " | " |
| IC 5 | TA7347P | " | " |
| IC 6 | – | – | |
| IC 7 | – | – | |
| IC 8 | – | – | |
| IC 9 | – | – | |
| IC10 | – | – | |
| IC11 | – | – | |
| IC12 | – | – | |
| IC13 | – | – | |
| IC14 | – | – | |
| IC15 | – | – | |
| IC16 | NJM1496D | IC (M) | JRC |
| IC17 | TA7347P | " | TOSHIBA |
| IC18 | NJM1496D | " | JRC |
| IC19 | " | " | " |
| IC20 | – | – | |
| IC21 | – | – | |
| IC22 | – | – | |
| IC23 | TC4049BP | IC (M) | TOSHIBA |
| IC24 | HA11720 | " | HITACHI |
| IC25 | – | – | |
| IC26 | – | – | |
| IC27 | NJM311D | IC (M) | JRC |
| IC28 | TC40H002P | " | TOSHIBA |
| IC29 | HA11720 | " | HITACHI |
| IC30 | TC4053BP | " | TOSHIBA |
| IC31 | – | – | |
| IC32 | – | – | |
| IC33 | – | – | |
| IC34 | – | – | |
| IC35 | HA13002 | IC (M) | HITACHI |
| IC36 | NJM5534D | " | JRC |
| IC37 | " | " | " |
| IC38 | TA78L005AP | " | TOSHIBA |
| IC39 | NJM79L05A | " | JRC |
| IC40 | TC4049BP | " | TOSHIBA |
| Q 1 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q 2 | " | " | " |
| Q 3 | " | " | " |
| Q 4 | " | " | " |
| Q 5 | " | " | " |
| Q 6 | 2SC2812L5.6 | Si. Transistor | SANYO |
| Q 7 | " | " | " |
| Q 8 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q 9 | 2SA1256E4.5 | Si. Transistor | SANYO |
| Q10 | 2SC2814F4.5 | " | " |
| Q11 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q12 | 2SA1256E4.5 | Si. Transistor | SANYO |
| Q13 | 2SC2814F4.5 | " | " |
| Q14 | " | " | " |
| Q15 | " | " | " |
| Q16 | – | – | |
| Q17 | 2SC2814F4.5 | Si. Transistor | SANYO |
| Q18 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q19 | 2SA1256E4.5 | Si. Transistor | SANYO |
| Q20 | 2SC2814F4.5 | " | " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| Q21 | 2SC2814F4.5 | Si. Transistor | SANYO |
| Q22 | " | " | " |
| Q23 | 2SC2812L5.6 | " | " |
| Q24 | – | – | |
| Q25 | 2SA1256E4.5 | Si. Transistor | SANYO |
| Q26 | " | " | " |
| Q27 | 2SC2814F4.5 | " | " |
| Q28 | 2SC2812L5.6 | " | " |
| Q29 | 2SC2814F4.5 | " | " |
| Q30 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q31 | 2SA1256E4.5 | Si. Transistor | SANYO |
| Q32 | 2SC2814F4.5 | " | " |
| Q33 | " | " | " |
| Q34 | 2SA1256E4.5 | " | " |
| Q35 | 2SC2814F4.5 | " | " |
| Q36 | 2SA1256E4.5 | " | " |
| Q37 | 2SC2814F4.5 | " | " |
| Q38 | " | " | " |
| Q39 | " | " | " |
| Q40 | 2SA1256E4.5 | " | " |
| Q41 | 2SC2812L5.6 | " | " |
| Q42 | 2SC2814F4.5 | " | " |
| Q43 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q44 | 2SC2814F4.5 | Si. Transistor | SANYO |
| Q45 | 2SA1256E4.5 | " | " |
| Q46 | 2SC2814F4.5 | " | " |
| Q47 | 2SA1256E4.5 | " | " |
| Q48 | 2SC2814F4.5 | " | " |
| Q49 | " | " | " |
| Q50 | " | " | " |
| Q51 | " | " | " |
| Q52 | " | " | " |
| Q53 | " | " | " |
| Q54 | 2SA1256E4.5 | " | " |
| Q55 | " | " | " |
| Q56 | " | " | " |
| Q57 | " | " | " |
| Q58 | " | " | " |
| Q59 | 2SC2812L5.6 | " | " |
| Q60 | " | " | " |
| Q61 | " | " | " |
| Q62 | " | " | " |
| Q63 | 2SA1256E4.5 | " | " |
| Q64 | 2SC2814F4.5 | " | " |
| Q65 | " | " | " |
| Q66 | " | " | " |
| Q67 | 2SC2812L5.6 | " | " |
| Q68 | " | " | " |
| Q69 | 2SA1012(Y) | " | TOSHIBA |
| Q70 | 2SA1179M5.6 | " | SANYO |
| Q71 | 2SC2812L5.6 | " | " |
| Q72 | " | " | " |
| Q73 | 2SA1020(Y) | " | TOSHIBA |
| Q74 | " | " | " |
| Q75 | " | " | " |
| Q76 | 2SC2812L5.6 | " | SANYO |
| Q77 | 2SC2655(Y) | " | TOSHIBA |
| Q78 | – | – | |
| Q79 | – | – | |
| Q80 | 2SA1012(Y) | Si. Transistor | TOSHIBA |
| Q81 | 2SC2814F4.5 | " | SANYO |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| D 1 | MA152K | Si. Diode | MATSUSHITA |
| D 2 | " | " | " |
| D 3 | HZ9A2L | Ze. Diode | 9 V HITACHI |
| D 4 | " | " | " " |
| D 5 | " | " | " " |
| D 6 | MA152K | Si. Diode | MATSUSHITA |
| D 7 | " | " | " |
| D 8 | " | " | " |
| D 9 | " | " | " |
| D10 | " | " | " |
| D11 | " | " | " |
| D12 | " | " | " |
| D13 | " | " | " |
| D14 | HZ15-3L | Ze. Diode | 15 V HITACHI |
| D15 | " | " | " " |
| D16 | " | " | " " |
| D17 | S4VB20 | Si. Diode | |
| D18 | DS135TE | " | SANYO |
| D19 | ERC81-004 | " | |
| D20 | " | " | |
| D21 | " | " | |
| D22 | MA152K | " | MATSUSHITA |
| D23 | " | " | " |
| C 1 | QER41CM-476 | E Cap | 47 16 V |
| C 2 | " -476 | " | 47 " |
| C 3 | " -476 | " | 47 " |
| C 4 | " -476 | " | 47 " |
| C 5 | " -476 | " | 47 " |
| C 6 | QCS81HJ-150 | C Cap | 15 P 50 V J |
| C 7 | QEPA1HM-105 | E Cap | 1 " |
| C 8 | QCS81HJ-150 | C Cap | 15 P " J |
| C 9 | QEPA1HM-105 | E Cap | 1 " |
| C10 | QCS81HJ-150 | C Cap | 15 P " J |
| C11 | QEPA1HM-105 | E Cap | 1 " |
| C12 | QCS81HJ-150 | C Cap | 15 P " J |
| C13 | QEPA1HM-105 | E Cap | 1 " |
| C14 | QCS81HJ-150 | C Cap | 15 P " J |
| C15 | QEPA1HM-105 | E Cap | 1 " |
| C16 | QER41CM-476 | " | 47 16 V |
| C17 | " -476 | " | 47 " |
| C18 | " -476 | " | 47 " |
| C19 | " -476 | " | 47 " |
| C20 | " -476 | " | 47 " |
| C21 | " -476 | " | 47 " |
| C22 | – | – | |
| C23 | QER41EM-106 | E Cap | 10 25 V |
| C24 | " -106 | " | 10 " |
| C25 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C26 | QCF81HZ-104 | " | 0.1 " |
| C27 | QER41CM-476 | E Cap | 47 16 V |
| C28 | " -476 | " | 47 " |
| C29 | " -476 | " | 47 " |
| C30 | QER41EM-106 | " | 10 25 V |
| C31 | QEX41EM-334 | " | 0.33 " |
| C32 | QCS81HJ-150 | C Cap | 15 P 50 V J |
| C33 | QER41CM-476 | E Cap | 47 16 V |
| C34 | QEX41EM-334 | " | 0.33 25 V |
| C35 | QCS81HJ-150 | C Cap | 15 P 50 V J |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| C36 | QER41CM-476 | E Cap | 47 16 V |
| C37 | " -476 | " | 47 " |
| C38 | " -476 | " | 47 " |
| C39 | QER41EM-106 | " | 10 25 V |
| C40 | " -106 | " | 10 " |
| C41 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C42 | QCF81HZ-104 | " | 0.1 " |
| C43 | QER41CM-476 | E Cap | 47 16 V |
| C44 | QEE41VM-104 | T Cap | 0.1 35 V |
| C45 | QCS81HJ-150 | C Cap | 15 P 50 V J |
| C46 | QER41CM-476 | E Cap | 47 16 V |
| C47 | " -476 | " | 47 " |
| C48 | " -476 | " | 47 " |
| C49 | QCS81HJ-5R0 | C Cap | 5 P 50 V J |
| C50 | " -5R0 | " | 5 P " " |
| C51 | QER41CM-476 | E Cap | 47 16 V |
| C52 | " -476 | " | 47 " |
| C53 | " -476 | " | 47 " |
| C54 | QEPA1HM-105 | " | 1 50 V |
| C55 | QCS81HJ-150 | C Cap | 15 P " J |
| C56 | QEX41CM-156 | E Cap | 15 16 V |
| C57 | QER41CM-106 | " | 10 " |
| C58 | " -106 | " | 10 " |
| C59 | QETA1EM-106 | " | 10 " |
| C60 | " -476 | " | 47 " |
| C61 | " -476 | " | 47 " |
| C62 | " -476 | " | 47 " |
| C63 | " -476 | " | 47 " |
| C64 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C65 | " -104 | " | 0.1 " |
| C66 | " -104 | " | 0.1 " |
| C67 | QCY81HK-103 | " | 0.01 " K |
| C68 | " -103 | " | 0.01 " " |
| C69 | QER41EM-106 | E Cap | 10 25 V |
| C70 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C71 | QER41CM-476 | E Cap | 47 16 V |
| C72 | QCS81HJ-680 | C Cap (NTSC) | 68 P 50 V J |
| " | " -470 | " (PAL) | 47 P " " |
| C73 | " -100 | " | 10 P " " |
| C74 | " -100 | " | 10 P " " |
| C75 | " -101 | " | 100 P " " |
| C76 | " -330 | " | 33 P " " |
| C77 | " -180 | " | 18 P " " |
| C78 | QER41CM-476 | E Cap | 47 16 V |
| C79 | " -476 | " | 47 " |
| C80 | " -476 | " | 47 " |
| C81 | " -476 | " | 47 " |
| C82 | " -476 | " | 47 " |
| C83 | QEPA1HM-105 | " | 1 50 V |
| C84 | QCS81HJ-150 | C Cap | 15 P " J |
| C85 | QER41CM-476 | E Cap | 47 16 V |
| C86 | QCY81HK-103 | C Cap (NTSC) | 0.01 50 V K |
| C87 | QER41CM-476 | E Cap | 47 16 V |
| C88 | " -476 | " | 47 " |
| C89 | QCS81HJ-560 | C Cap (NTSC) | 56 P 50 V J |
| C90 | " -330 | " | 33 P " " |
| C91 | QER41CM-476 | E Cap | 47 16 V |
| C92 | QCS81HJ-560 | C Cap (NTSC) | 56 P 50 V J |
| C93 | " -330 | " | 33 P " " |
| C94 | QCF81HZ-104 | " | 0.1 " |
| C95 | " -104 | " | 0.1 " |
| C96 | " -104 | " | 0.1 " |
| C97 | QCY81HK-103 | " | 0.01 " K |
| C98 | " -103 | " | 0.01 " " |
| C99 | QCF81HZ-104 | " | 0.1 " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| C100 | QER41CM-476 | E Cap | 47 16 V |
| C101 | QER41EM-106 | " | 10 25 V |
| C102 | QCS81HJ-560 | C Cap (NTSC) | 56 P 50 V J |
| " | " -390 | " (PAL) | 39 P " " |
| C103 | " -121 | " (NTSC) | 120 P " " |
| " | " -680 | " (PAL) | 68 P " " |
| C104 | " -101 | " (NTSC) | 100 P " " |
| " | " -180 | " (PAL) | 18 P " " |
| C105 | " -221 | " (NTSC) | 220 P " " |
| " | " -150 | " (PAL) | 15 P " " |
| C106 | " -330 | " | 33 P " " |
| C107 | " -330 | " | 33 P " " |
| C108 | QCY81HK-103 | " | 0.01 " K |
| C109 | QCS81HJ-330 | " | 33 P " J |
| C110 | " -150 | " (NTSC) | 15 P " " |
| C110 | " -7R0 | " (PAL) | 7 P " " |
| C111 | QAT3001-011 | TR Cap | QUAD. PHASE |
| C112 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C113 | QER41CM-476 | E Cap | 47 16 V |
| C114 | QCS81HJ-560 | C Cap | 56 P 50 V J |
| C115 | " -680 | " | 68 P " " |
| C116 | " -151 | " | 150 P " " |
| C117 | " -151 | " | 150 P " " |
| C118 | " -151 | " | 150 P " " |
| C119 | " -680 | " | 68 P " " |
| C120 | " -220 | " | 22 P " " |
| C121 | " -120 | " | 12 P " " |
| C122 | QER41CM-476 | E Cap | 47 16 V |
| C123 | QCS81HJ-560 | C Cap (NTSC) | 56 P 50 V J |
| C124 | " -121 | " | 120 P " " |
| C125 | " -121 | " | 120 P " " |
| C126 | " -121 | " | 120 P " " |
| C127 | " -560 | " (NTSC) | 56 P " " |
| C128 | QER41CM-476 | E Cap | 47 16 V |
| C129 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C130 | " -103 | " | 0.01 " " |
| C131 | QCS81HJ-560 | " (NTSC) | 56 P " J |
| " | " -390 | " (PAL) | 39 P " " |
| C132 | " -101 | " (NTSC) | 100 P " " |
| " | " -330 | " (PAL) | 33 P " " |
| C133 | " -101 | " (NTSC) | 100 P " " |
| " | " -180 | " (PAL) | 18 P " " |
| C134 | " -151 | " (NTSC) | 150 P " " |
| " | " -121 | " (PAL) | 120 P " " |
| C135 | QER41CM-476 | E Cap | 47 16 V |
| C136 | " -476 | " | 47 " |
| C137 | " -476 | " | 47 " |
| C138 | " -476 | " | 47 " |
| C139 | " -476 | " | 47 " |
| C140 | " -476 | " | 47 " |
| C141 | " -476 | " | 47 " |
| C142 | " -476 | " | 47 " |
| C143 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C144 | QCS81HJ-680 | " | 68 P " J |
| C145 | QEV71ER-478 | E Cap | 4700 25 V |
| C146 | QER41EM-336 | " | 33 " |
| C147 | " -336 | " | 33 " |
| C148 | " -336 | " | 33 " |
| C149 | " -336 | " | 33 " |
| C150 | QCS81HJ-221 | C Cap | 220 P 50 V J |
| C151 | QCF81HZ-104 | " | 0.1 " |
| C152 | QCS81HJ-152 | " | 0.0015 " J |
| C153 | QEX41CM-156 | E Cap | 15 16 V |
| C154 | QER41CM-476 | " | 47 " |
| C155 | " -476 | " | 47 " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| C156 | QER41CM-476 | E Cap | 47 16 V |
| C157 | " -476 | " | 47 " |
| C158 | " -476 | " | 47 " |
| C159 | " -476 | " (PAL) | 47 " |
| C160 | QER41EM-336 | " | 33 25 V |
| C161 | " -336 | " | 33 " |
| C162 | " -336 | " | 33 " |
| C163 | QEX41CM-156 | " (NTSC) | 15 16 V |
| " | QER41CM-476 | " (PAL) | 47 " |
| C164 | QETA1CM-107 | " (NTSC) | 100 " |
| " | QER41CM-476 | " (PAL) | 47 " |
| C165 | QETA1CM-107 | " (NTSC) | 100 " |
| " | QER41CM-476 | " (PAL) | 47 " |
| C166 | QEX41CM-156 | " | 15 " |
| C167 | QETA1CM-107 | " | 100 " |
| C168 | " -107 | " | 100 " |
| C169 | QCY81HK-223 | C Cap (NTSC) | 0.022 50 V K |
| C170 | QER41EM-106 | E Cap | 10 25 V |
| C171 | " -106 | " | 10 " |
| C172 | QER41CM-476 | " | 47 16 V |
| C173 | " -476 | " | 47 " |
| C174 | " -476 | " | 47 " |
| C175 | QCS81HJ-102 | C Cap (NTSC) | 0.001 50 V J |
| C176 | QEX41CM-156 | E Cap | 15 16 V |
| C177 | QET41CM-107 | " | 100 " |
| C178 | " -107 | " | 100 " |
| C179 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C180 | QER41CM-476 | E Cap | 47 16 V |
| C181 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C182 | QER41CM-476 | E Cap | 47 16 V |
| C183 | " -476 | " | 47 " |
| C184 | " -476 | " | 47 " |
| C185 | " -476 | " | 47 " |
| C186 | " -476 | " | 47 " |
| C187 | QCS81HJ-100 | C Cap | 10 P 50 V J |
| C188 | QCF81HZ-104 | " | 0.1 " |
| C189 | QCS81HJ-100 | " | 10 P " J |
| C190 | QCF81HZ-104 | " | 0.1 " |
| C191 | – | – | |
| C192 | QCS81HJ-150 | C Cap | 15 P 50 V J |
| C193 | " -150 | " | 15 P " " |
| C194 | " -150 | " | 15 P " " |
| C195 | QCF81HZ-104 | " | 0.1 " |
| C196 | " -104 | " | 0.1 " |
| C197 | QCS81HJ-270 | " | 27 P " J |
| C198 | – | – | |
| C199 | QCS81HJ-270 | C Cap (NTSC) | 27 P 50 V J |
| C200 | QER41EM-336 | E Cap | 33 25 V |
| C201 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C202 | QCF81HZ-104 | " | 0.1 " |
| C203 | – | – | |
| C204 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C205 | " -103 | " | 0.01 " " |
| C206 | " -103 | " | 0.01 " " |
| C207 | – | – | |
| C208 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C209 | – | – | |
| C210 | QEX41CM-156 | OS Cap | 15 10 V |
| C211 | QCS81HJ-680 | C Cap | 68 P 50 V J |
| C212 | QCS81HZ-104 | " | 0.1 " |
| C213 | QCY81HK-103 | " | 0.01 " |
| C214 | QCF81HZ-104 | " | 0.1 " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| R20 | SCV0491-501 | VR (500) | B-PHASE |
| R22 | SCV0491-102 | VR (1 K) | B-PEDESTAL |
| R26 | SCV0491-103 | VR (10 K) | DIF-BAL. |
| R34 | SCV0491-501 | VR (500) | B-GAIN |
| R36 | SCV0491-501 | VR (500) | A-GAIN |
| R51 | SCV0491-103 | VR (10 K) | DIF. BAL. |
| R57 | SCV0491-501 | VR (500) | D. PV-PED. |
| R59 | SCV0491-501 | VR (500) | D. PV-GAIN |
| R62 | SCV0491-501 | VR (500) | PGM-PHASE |
| R69 | SCV0491-501 | VR (500) | PGM-2 GAIN |
| R74 | SCV0491-103 | VR (10 K) | DIF. BAL. |
| R78 | SCV0491-501 | VR (500) | PVW-GAIN |
| R91 | SCV0491-501 | VR (500) | DSK-PED. |
| R93 | SCV0491-501 | VR (500) | PGM-1 GAIN |
| R105 | SCV0491-501 | VR (500) | BC-W-BAL. |
| R131 | SCV0491-501 | VR (500) | B.C. CHROMA |
| R162 | SCV0491-501 | VR (500) | DSK-W-BAL. |
| R192 | SCV0491-501 | VR (500) | DSK-CHROMA |
| R237 | SCV0491-103 | VR (10 K) | B.B. SYNC. |
| R240 | SCV0491-501 | VR (500) | B.B. BURST |
| R270 | SCV0491-102 | VR (1 K) | +9 V ADJ. |
| R295 | SCV0491-501 | VR (500) | B.C. PHASE |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| L 1 | SCV0331-820 | Peaking Coil | 82 μH |
| L 2 | " -820 | " | 82 μH |
| L 3 | " -820 | " | 82 μH |
| L 4 | " -820 | " | 82 μH |
| L 5 | " -820 | " | 82 μH |
| L 6 | " -820 | " | 82 μH |
| L 7 | " -820 | " | 82 μH |
| L 8 | " -820 | " | 82 μH |
| L 9 | " -2R2 | " | 2.2 μH |
| L10 | " -820 | " | 82 μH |
| L11 | " -820 | " | 82 μH |
| L12 | – | – | |
| L13 | SCV0331-820 | Peaking Coil | 82 μH |
| L14 | " -100 | " | 10 μH |
| L15 | " -220 | " (NTSC) | 22 μH |
| " | " -390 | " (PAL) | 39 μH |
| L16 | " -330 | " | 33 μH |
| L17 | " -330 | " | 33 μH |
| L18 | " -330 | " | 33 μH |
| L19 | " -330 | " | 33 μH |
| L20 | " -330 | " | 33 μH |
| L21 | " -330 | " | 33 μH |
| L22 | " -270 | " | 27 μH |
| L23 | " -270 | " | 27 μH |
| L24 | " -270 | " | 27 μH |
| L25 | " -270 | " | 27 μH |
| L26 | " -100 | " | 10 μH |
| L27 | " -220 | " (NTSC) | 22 μH |
| " | " -390 | " (PAL) | 39 μH |
| L28 | SSV0623 | Coil Ass'y | 300 μH |
| L29 | SCV0392-250 | Choke Coil | 250 μH |
| L30 | SCV0391-250 | " | 250 μH |
| L32 | SCV0391-250 | | 250 μH |
| F 1 | A44594-002 | Fuse Guide | |
| F 2 | " -002 | " | |
| | SS42487 | Heat Sink (for IC2430STL30) | |
| | SS31054-030 | C. Fit Connector | |
| | SCV0513-40S | Connector | |
| CN17 | SCV0440-004 | AUSV Header | |
| S 1 | SCV0490-001 | Slide Switch (Added) | POSI ⟷ NEGA |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| **• CBM-1** | **CBMC4070-00A** | **CP BOARD ASS'Y** | **Clamp** |
| **• CBM-2** | **" -00A** | **"** | **"** |
| **• CBM-3** | **" -00A** | **"** | **"** |
| **• CBM-4** | **" -00A** | **"** | **"** |
| **• CBM-5** | **" -00A** | **"** | **"** |
| Q 1 | 2SC2812L5.6 | Si. Transistor | SANYO |
| Q 2 | 2SA1179M5.6 | " | " |
| Q 3 | 2SC2812L5.6 | " | " |
| Q 4 | " | " | " |
| Q 5 | " | " | " |
| Q 6 | " | " | " |
| D 1 | MA152K | Si. Diode | MATSUSHITA |
| D 2 | " | " | " |
| D 3 | " | " | " |
| D 4 | " | " | " |
| C 1 | QCF81HZ-104 | C Cap | 0.1 50 V |
| | SCV0741-007 | H.I.C. Header | 7 Pin |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| **• CBM-6** | **CBMC4073-00A** | **BA-1 BOARD ASS'Y** | **Buffer** |
| **• CBM-7** | **" -00B** | **BA-2 BOARD ASS'Y** | **"** |
| **• CBM-8** | **" -00B** | **"** | **"** |
| **• CBM-9** | **" -00A** | **BA-1 BOARD ASS'Y** | **"** |

*** Difference point between "-00A" and "-00B"**

| | -00A | -00B |
|---|---|---|
| R 5 | 270 Ω | OPEN |

Other parts are common as follows.

| | | | |
|---|---|---|---|
| Q 1 | 2SC2814F4.5TA | Si. Transistor | SANYO |
| Q 2 | " | " | " |
| Q 3 | 2SA1256E4.5TB | " | " |
| C 1 | QCY81HK-103Z | C Cap | 0.01 50 V |
| C 2 | QCS81HJ-330Z | " | 33 P " J |
| C 3 | " -7R0Z | " | 7 P " " |
| C 4 | QCF81HZ-104Z | " | 0.1 " |
| | SCV0741-007 | H.I.C. Header | 7 Pin |

"Revised on June 1989"

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| • CBM-10 | CBMC4071-00B | VA-2 BOARD ASS'Y | Video Amp |
| • CBM-11 | " -00A | VA-1 BOARD ASS'Y | " |
| • CBM-12 | " -00A | " | " |
| • CBM-13 | " -00A | " | " |
| • CBM-16 | " --00A | " | " |
| • CBM-17 | " -00A | " | " |
| • CBM-18 | " -00A | " | " |

* Difference point between "-00A" and "-00B"

| | -00A | -00B |
|---|---|---|
| R 6 | 1 K | OPEN |

Other parts are common as follows

| | | | |
|---|---|---|---|
| Q 1 | 2SC2814F4.5 | Si. Transistor | SANYO |
| Q 2 | " | " | " |
| Q 3 | " | " | " |
| C 1 | QCF81HZ-104Z | C Cap | 0.1 50 V |
| C 2 | " -104Z | " | 0.1 " |
| | SCV0741-009 | H.I.C. Header | 9 Pin |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| • CBM-14 | CBMC4072-00B | PA-2 BOARD ASS'Y | Pulse Amp |
| • CBM-15 | " -00A | PA-1 BOARD ASS'Y | " |
| • CBM-19 | " -00A | " | " |

* Difference point between "-00A" and "-00B"

| | -00A | -00B |
|---|---|---|
| R 1 | 6.8 K | 5.6 K |
| R 2 | 22 K | 15 K |

Other parts are common as follows

| | | | |
|---|---|---|---|
| Q 1 | 2SA1179M5.6 | Si. Transistor | SANYO |
| Q 2 | " | " | " |
| Q 3 | " | " | " |
| Q 4 | " | " | " |
| C 1 | QCF81HZ-104Z | C Cap | 0.1 50 V |
| | SCV0741-007 | H.I.C. Header | 7 Pin |

## 6.2 WG BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| IC 1 | – | – | |
| IC 2 | – | – | |
| IC 3 | – | – | |
| IC 4 | TC4049BP | IC (M) | TOSHIBA |
| IC 5 | – | – | |
| IC 6 | TC4053BP | IC (M) | TOSHIBA |
| IC 7 | HA11247 | " | HITACHI |
| IC 8 | NJM4560D | " | JRC |
| IC 9 | HD44007A | " | HITACHI |
| IC10 | TC40H000P | " | TOSHIBA |
| IC11 | AN612 | " (PAL) | MATSUSHITA |
| IC12 | " | " (PAL) | " |
| IC13 | SCV0533-001 | Function Module (H) | (PAL) JVC |
| IC14 | BA634 | IC (M) (PAL) | ROHM |
| IC15 | SCV0267-001 | Function Module(H) | (PAL) JVC |
| IC16 | BA634 | IC (M) (PAL) | ROHM |
| IC17 | NJM4560D | " | JRC |
| IC18 | TL062CP | " | TEXAS |
| IC19 | TC4053BP | " | TOSHIBA |
| IC20 | LF357N | " | MOTOROLA |
| IC21 | TL062CP | " | TEXAS |
| IC22 | TC4053BP | " | TOSHIBA |
| IC23 | LF356N | " | MOTOROLA |
| IC24 | TC4051BP | " | TOSHIBA |
| IC25 | NJM311D | " | JRC |
| IC26 | TC4049BP | " | TOSHIBA |
| Q 1 | 2SC2814F4.5 | Transistor | SANYO |
| Q 2 | – | – | |
| Q 3 | – | – | |
| Q 4 | – | – | |
| Q 5 | – | – | |
| Q 6 | – | – | |
| Q 7 | – | – | |
| Q 8 | – | – | |
| Q 9 | – | – | |
| Q10 | – | – | |
| Q11 | – | – | |
| Q12 | 2SC2812L5.6 | Transistor | SANYO |
| Q13 | 2SA1179M5.6 | " | " |
| Q14 | 2SC2814F4.5 | " | " |
| Q15 | " | " | " |
| Q16 | " | " (PAL) | " |
| Q17 | 2SC2812L5.6 | " | " |
| Q18 | 2SC2814F4.5 | " | " |
| Q19 | 2SA1179M5.6 | " (PAL) | " |
| Q20 | 2SC2814F4.5 | " (PAL) | " |
| Q21 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q22 | 2SA1179M5.6 | Transistor | SANYO |
| Q23 | " | " | " |
| Q24 | " | " | " |
| Q25 | " | " | " |
| Q26 | 2SC2812L5.6 | " | " |
| Q27 | 2SK198(Q,R) | FET | MATSUSHITA |
| Q28 | – | – | |
| Q29 | 2SC2814F4.5 | Transistor | SANYO |
| Q30 | " | " | " |
| Q31 | 2SA1256E4.5 | " | " |
| Q32 | 2SC2812L5.6 | " | " |
| Q33 | " | " | " |
| Q34 | " | " | " |
| Q35 | 2SC2814F4.5 | " | " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| Q36 | 2SC2814F4.5 | Transistor | SANYO |
| Q37 | 2SA1256E4.5 | " | " |
| Q38 | 2SK198(Q,R) | FET | MATSUSHITA |
| D 1 | MA152K | Diode | MATSUSHITA |
| D 2 | HZ3B2 | Ze. Diode | 3 V HITACHI |
| D 3 | SVC321(A) | V.C. Diode | |
| D 4 | " | " (PAL) | |
| D 5 | " | " | |
| D 6 | – | – | |
| D 7 | – | – | |
| D 8 | – | – | |
| D 9 | MA152K | Diode | MATSUSHITA |
| D10 | " | " | " |
| D11 | " | " | " |
| D12 | " | " | " |
| D13 | " | " | " |
| D14 | " | " | " |
| D15 | " | " | " |
| D16 | " | " | " |
| D17 | – | – | |
| D18 | – | – | |
| D19 | SVC321(A) | V.C. Diode | |
| D20 | " | " | |
| D21 | " | " | |
| D22 | " | " | |
| D23 | MA152K | Diode | MATSUSHITA |
| D24 | 1S1555 | " | |
| C 1 | QEPA0JM-476 | E Cap | 47 6.3 V |
| C 2 | QER41HM-475 | " | 4.7 50 V |
| C 3 | QER41CM-476 | " | 47 16 V |
| C 4 | QER41EM-106 | " | 10 25 V |
| C 5 | QCS81HJ-560 | C Cap | 56 P 50 V J |
| C 6 | – | – | |
| C 7 | – | – | |
| C 8 | – | – | |
| C 9 | – | – | |
| C10 | – | – | |
| C11 | – | – | |
| C12 | QER41CM-476 | E Cap | 47 6.3 V |
| C13 | QCF81HZ-104 | C Cap | 0.01 50 V |
| C14 | QCS81HJ-101 | " | 100 P " J |
| C15 | – | – | |
| C16 | – | – | |
| C17 | QCS81HJ-101 | C Cap | 100 P 50 V J |
| C18 | " -101 | " | 100 P " " |
| C19 | – | – | |
| C20 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C21 | QCS81HJ-101 | " | 100 P " J |
| C22 | " -101 | " | 100 P " " |
| C23 | " -101 | " | 100 P " " |
| C24 | " -121 | " | 120 P " " |
| C25 | QCF81HZ-104 | " | 0.1 " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| C26 | QER41CM-476 | E Cap | 47 16 V |
| C27 | QCS81HJ-470 | C Cap (NTSC) | 47 P 50 V J |
| " | " -330 | " (PAL) | 33 P " " |
| C28 | QCY81HK-103 | " | 0.01 " K |
| C29 | QCS81HJ-560 | " (PAL) | 56 P " J |
| C30 | " -560 | " (PAL) | 56 P " " |
| C31 | QCY81HK-103 | " | 0.01 " K |
| C32 | QER41CM-476 | E Cap | 47 16 V |
| C33 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C34 | QEPA1HM-105 | NP Cap | 1 " |
| C35 | QCS81CH-101 | C Cap | 100 P 16 V |
| C36 | QCY81HK-103 | " | 0.01 50 V K |
| C37 | " -333 | " | 0.033 " " |
| C38 | QER41HM-475 | E Cap | 4.7 " |
| C39 | QER41EM-106 | " | 10 25 V |
| C40 | QER41CM-476 | " | 47 16 V |
| C41 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C42 | QCS81HJ-151 | " | 150 P " J |
| C43 | QAT3001-011 | TR Cap | |
| C44 | QCS81HJ-7R0 | C Cap | 7 P 50 V J |
| C45 | QEPA1AM-106 | NP Cap | 10 10 V |
| C46 | QCS81HJ-102 | C Cap | 0.001 50 V J |
| C47 | QCF81HZ-104 | " | 0.1 " |
| C48 | QER41EM-106 | E Cap | 1 25 V |
| C49 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C50 | " -104 | " | 0.1 " |
| C51 | QCY81HK-103 | " | 0.01 " K |
| C52 | QEN41HM-105 | E Cap | 1 " |
| C53 | QCS81HJ-151 | C Cap | 150 P " J |
| C54 | – | – | |
| C55 | QCS81HJ-151 | C Cap | 150 P 50 V J |
| C56 | " -101 | " | 100 P " " |
| C57 | " -470 | " | 47 P " " |
| C58 | QER41CM-476 | E Cap | 47 16 V |
| C59 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C60 | QCF81HZ-104 | " | 0.1 " |
| C61 | QER41CM-476 | E Cap (PAL) | 47 16 V |
| C62 | QCS81HJ-330 | C Cap (PAL) | 33 P 50 V J |
| C63 | QER41CM-476 | E Cap (PAL) | 47 16 V |
| C64 | " -476 | " (PAL) | 47 " |
| C65 | " -476 | " (PAL) | 47 " |
| C66 | QCY81HK-103 | C Cap (PAL) | 0.01 50 V K |
| C67 | " -103 | " (PAL) | 0.01 " " |
| C68 | QER41CM-476 | E Cap (PAL) | 47 16 V |
| C69 | " -476 | " (PAL) | 47 " |
| C70 | QCY81HK-103 | C Cap (PAL) | 0.01 50 V K |
| C71 | " -103 | " (PAL) | 0.01 " " |
| C72 | QCS81HJ-101 | " (PAL) | 100 P " J |
| C73 | " -102 | " (PAL) | 1000 P " " |
| C74 | QEPA1HM-105 | NP Cap (PAL) | 1 " |
| C75 | QER41CM-476 | " | 47 16 V |
| C76 | " -476 | " | 47 " |
| C77 | " -476 | " | 47 " |
| C78 | QCS81HJ-560 | C Cap | 56 P 50 V J |
| C79 | QFN31HJ-682 | MY Cap | 0.0068 " K |
| C80 | " -103 | " | 0.01 " " |
| C81 | QCS81HJ-221 | C Cap | 220 P " J |
| C82 | QCY81HK-103 | " | 0.01 " K |
| C83 | – | – | |
| C84 | QCS81HJ-102 | C Cap | 0.001 50 V J |
| C85 | – | – | |
| C86 | – | – | |
| C87 | QEX41EM-225 | E Cap | 2.2 25 V |
| C88 | " -225 | " | 2.2 " |
| C89 | – | – | |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| C90 | QEE41VM-224 | T Cap(35 V - 0.22) | 0.22 35 V |
| C91 | " -224 | " ( " ) | 0.22 " |
| C92 | QFN41HJ-103 | MY Cap | 0.01 50 V K |
| C93 | " -103 | " | 0.01 " " |
| C94 | – | – | |
| C95 | – | – | |
| C96 | QER41CM-476 | E Cap | 47 16 V |
| C97 | " -476 | " | 47 " |
| C98 | " -476 | " | 47 " |
| C99 | " -476 | " | 47 " |
| C100 | " -476 | " | 47 " |
| C101 | " -476 | " | 47 " |
| C102 | QCS81HJ-470 | C Cap | 47 P 50 V J |
| C103 | – | – | |
| C104 | QCS81HJ-101 | C Cap | 100 P 50 V J |
| C105 | " -101 | " | 100 P " " |
| C106 | " -101 | " | 100 P " " |
| C107 | " -101 | " | 100 P " " |
| C108 | " -101 | " | 100 P " " |
| C109 | QCF81HZ-104 | " | 0.1 " |
| C110 | QER41CM-476 | E Cap | 47 16 V |
| C111 | QEPA1HM-105 | NP Cap | 1 50 V |
| C112 | QER41CM-476 | E Cap | 47 16 V |
| C113 | QCY81HK-103 | C Cap | 0.01 50 V K |
| C114 | QER41EM-106 | E Cap | 10 25 V |
| C115 | QCS81HJ-101 | C Cap | 100 P 50 V J |
| C116 | " -101 | " | 100 P " " |
| C117 | QER41CM-476 | E Cap | 47 16 V |
| C118 | QEPA1HM-105 | NP Cap | 1 50 V |
| C119 | " -105 | E Cap | 1 " |
| C120 | QEPA0HM-476 | NP Cap | 47 |
| C121 | QCS81HJ-151 | C Cap | 150 P 50 V J |
| C122 | " -7R0 | " | 7 P " " |
| C123 | QAT3001-011 | TR Cap | |
| C124 | QCS81HJ-271 | C Cap | 270 P 50 V J |
| C125 | " -150 | " | 15 P " " |
| C126 | QER41EM-106 | E Cap | 10 25 V |
| R29 | SCV0491-103 | VR (10 K) | H. PHASE |
| R52 | SCV0491-202 | VR (2 K) (PAL) | PAL ALT PHASE |
| R62 | SCV0491-102 | VR (1 K) | SC LOCK |
| R94 | QRV141F-6801AY | M.F.R. | 6.8 K 1/4 W |
| R95 | " -6801AY | " | 6.8 K " |
| R99 | " -1502AY | " | 15 K " |
| R100 | " -1002AY | " | 10 K " |
| R102 | SCV0491-203 | VR (20 K) | H. SAW-LEVEL |
| R107 | SCV0491-203 | VR (20 K) | H. PARA-LEVEL |
| R131 | SCV0491-503 | VR (50 K) | V. SAW-LEVEL |
| R136 | SCV0491-503 | VR (50 K) | V. PARA-LEVEL |
| R142 | SCV0491-103 | VR (10 K) | INV. DC |
| R156 | SCV0491-502 | VR (5 K) | MIX DC |
| R168 | SCV0491-501 | VR (500) | W. BAL. |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| R181 | SCV0515-202 | VR (2 K) | KEY SLICE |
| R187 | SCV0515-202 | VR (2 K) | DSK SLICE |
| R191 | SCV0515-202 | VR (2 K) | DSK LEVEL |
| L 1 | – | – | |
| L 2 | SCV0331-390 | Peaking Coil | 39 μH |
| L 3 | " -220 | " | 22 μH |
| L 4 | " -120 | " | 12 μH |
| L 5 | " -100 | " | 10 μH |
| L 6 | SCV0100-001 | Coil | |
| L 7 | SCV0331-120 | Peaking Coil (PAL) | 12 μH |
| L 8 | – | – | |
| L 9 | SCV0331-220 | Peaking Coil(NTSC) | 22 μH |
| L10 | " -220 | " ( " ) | 22 μH |
| L11 | " -220 | " ( " ) | 22 μH |
| L12 | " -220 | " ( " ) | 22 μH |
| L13 | " -220 | " ( " ) | 22 μH |
| L14 | " -220 | " | 22 μH |
| L15 | " -220 | " | 22 μH |
| L16 | " -220 | " | 22 μH |
| L17 | " -220 | " | 22 μH |
| L18 | " -100 | " | 10 μH |
| L19 | " -150 | " | 15 μH |
| X'TAL 1 | SCV0349-001 | Crystal (PAL) | |
| X'TAL 2 | SCV0347-001 | " (NTSC) | |
| X'TAL 2 | SCV0348-001 | " (PAL) | |
| T 1 | GC44286-001 | SC. Trans. | |
| T 1 | SCV0171-001 | Transformer (PAL) | |
| T 2 | " -001 | " (PAL) | |
| S 1 | SCV0517-101 | BCD Switch | DSK COLOR |
| S 2 | SCV0656-023-6S | S. Switch | SC PHASE |
| CN20 | SCV0495-012 | Connector | 12 Pin |
| CN21 | " -012 | " | 12 Pin |
| CN22 | SS31054-014 | C. Fit Connector | 14 Pin |
| CN23 | " -030 | " | 30 Pin |
| CN24 | SCV0440-004 | Connector | 4 Pin |
| CN25 | – | – | |
| CN26 | SCV0495-008 | Connector | 8 Pin |

"Revised on June 1989"

## 6.3 CO BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| IC 1 | TC4532BP | IC (M) | TOSHIBA |
| IC 2 | TC4042BP | " | " |
| IC 3 | TC4028BP | " | " |
| IC 4 | TC4049BP | " | " |
| IC 5 | TC4011BP | " | " |
| IC 6 | TC4093BP | " | " |
| IC 7 | TC4013BP | " | " |
| IC 8 | TC4538BP | " | " |
| IC 9 | " | " | " |
| Q 1 | 2SC2812L5.6 | Si. Transistor | SANYO |
| Q 2 | " | " | " |
| Q 3 | 2SA1256E4.5 | " | " |
| Q 4 | 2SC2814F4.5 | " | " |
| Q 5 | 2SC2812L5.6 | " | " |
| Q 6 | " | " | " |
| Q 7 | 2SC2814F4.5 | " | " |
| Q 8 | " | " | " |
| Q 9 | 2SA1256E4.5 | " | " |
| Q10 | 2SC2814F4.5 | " | " |
| Q11 | 2SA1256E4.5 | " | " |
| Q12 | 2SC2814F4.5 | " | " |
| Q13 | " | " | " |
| D 1 | MA152K | Si. Diode | MATSUSHITA |
| D 2 | " | " | " |
| D 3 | " | " | " |
| D 4 | " | " | " |
| D 5 | " | " | " |
| D 6 | " | " | " |
| D 7 | " | " | " |
| D 8 | " | " | " |
| D 9 | " | " | " |
| D10 | " | " | " |
| D11 | " | " | " |
| D12 | " | " | " |
| D13 | " | " | " |
| C 1 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C 2 | QCS81HJ-101 | " | 0.1 " J |
| C 3 | QCF81HZ-104 | " | 0.1 " |
| C 4 | QCS81HJ-560 | " | 56 P " J |
| C 5 | QCF81HZ-104 | " | 0.1 " |
| C 6 | " -104 | " | 0.1 " |
| C 7 | " -104 | " | 0.1 " |
| C 8 | " -104 | " | 0.1 " |
| C 9 | " -104 | " | 0.1 " |
| C10 | QEE41CM-685 | T Cap | 6.8 1 V |
| C11 | QCS81HJ-470 | C Cap | 47 P 50 V J |
| C12 | QCF81HZ-104 | " | 0.1 " |
| C13 | QEE41VM-224 | T Cap (35 V - 0.22) | 0.22 35 V |
| C14 | QCS81HZ-820Z | C Cap | 82 P 50 V |
| C15 | QCF81HZ-104Z | " | 0.1 " |

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| C16 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C17 | " -104 | " | 0.1 " |
| C18 | " -104 | " | 0.1 " |
| C19 | " -104 | " | 0.1 " |
| C20 | QCY81HK-102 | " | 0.001 " K |
| C21 | " -103 | " | 0.01 " " |
| C22 | QCS81HJ-220 | " | 22 P " J |
| C23 | " -220 | " | 22 P " " |
| C24 | QCF81HZ-104 | " | 0.1 " |
| C25 | QCS81HJ-270 | " | 27 P " J |
| C26 | " -270 | " | 27 P " " |
| C27 | QCY81HK-103 | " | 0.01 " K |
| C28 | " -103 | " | 0.01 " " |
| R17 | SCV0491-202 | VR (2 K) | SC PHASE |
| R29 | SCV0491-103 | VR (10 K) | KEY DELAY |
| CN 1 | SCV0494-008 | Connector | 8 Pin |
| CN20 | SCV0494-012 | Connector | 12 Pin |
| CN21 | " -012 | " | 12 Pin |
| S1 to S10 : Refer to "Sec. 4 Exploded View and Parts List". | | | |

## 6.4 LO BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| IC 1 | TC4042BP | IC (M) | TOSHIBA |
| IC 2 | " | " | " |
| IC 3 | " | " | " |
| IC 4 | " | " | " |
| IC 5 | TC4022BP | " | " |
| IC 6 | TC4051BP | " | " |
| IC 7 | " | " | " |
| IC 8 | " | " | " |
| IC 9 | TD62306P | " | " |
| IC10 | TC4011BP | " | " |
| IC11 | " | " | " |
| IC12 | " | " | " |
| IC13 | TC4049BP | " | " |
| IC14 | NJM4558D | " | JRC |
| IC15 | TC4028BP | " | TOSHIBA |
| IC16 | NJM2903D | " | JRC |
| Q 1 | 2SA1179M5.6 | Si. Transistor | SANYO |
| Q 2 | " | " | " |
| D 1 | MA152K | Si. Diode | MATSUSHITA |
| D 2 | " | " | " |
| D 3 | " | " | " |
| D 4 | " | " | " |
| D 5 | " | " | " |
| D 6 | " | " | " |
| D 7 | GL-5HD22 | LED | |
| D 8 | " | " | |
| D 9 | " | " | |
| D10 | " | " | |
| D11 | " | " | |
| D12 | " | " | |
| D13 | " | " | |
| D14 | MA152K | Diode | |
| D15 | " | " | |
| C 1 | QER41CM-476 | E Cap | 47 16 V |
| C 2 | QCS81HJ-101 | C Cap | 100 P 50 V J |
| C 3 | " -101 | " | 100 P " " |
| C 4 | " -101 | " | 100 P " " |
| C 5 | " -101 | " | 100 P " " |
| C 6 | QER41CM-476 | E Cap | 47 16 V |
| C 7 | " -476 | " | 47 " |
| C 8 | " -476 | " | 47 " |
| R20 | SCV0492-502 | VR (5 K) | FADER-HI |
| R23 | SCV0492-502 | VR (5 K) | FADER-LOW |
| S 1 | SCV0517-101 | Switch | BACK COLOR |
| CN 1 | SCV0495-012 | Connector | 12 Pin |
| CN 2 | " -012 | " | 12 Pin |
| | SCV0441-003 | " | 3 Pin |
| | " -004 | " | 4 Pin |
| | SS31053-014 | C. Fit Connector | 14 Pin |
| CN 6 | " -030 | " | 30 Pin |

## 6.5 SW BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| IC 1 | TC4028BP | IC (M) | TOSHIBA |
| IC 2 | " | " | " |
| IC 3 | " | " | " |
| IC 4 | TC4532BP | " | " |
| IC 5 | TC4049BP | " | " |
| IC 6 | " | " | " |
| IC 7 | " | " | " |
| Q 1 | 2SA1179M5.6 | Si. Transistor | SANYO |
| Q 2 | " | " | " |
| D 1 | MA152K | Si. Diode | MATSUSHITA |
| D 2 | " | " | " |
| D 3 | " | " | " |
| D 4 | " | " | " |
| D 5 | " | " | " |
| D 6 | " | " | " |
| D 7 | " | " | " |
| C 1 | QCF81HZ-104 | C Cap | 0.1 50 V |
| C 2 | " -104 | " | 0.1 " |
| C 3 | " -104 | " | 0.1 " |
| CN 1 | SCV0494-012 | Connector | 12 Pin |
| CN 2 | " -012 | " | 12 Pin |
| S1 to S17 : Refer to "Sec. 4 Exploded View and Parts List". | | | |

## 6.6 BT BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| R 1 | QRV141F-75R0A | MFR | 75 1/4 W |
| R 2 | " -75R0A | " | 75 " |
| R 3 | " -75R0A | " | 75 " |
| R 4 | " -75R0A | " | 75 " |
| R 5 | " -75R0A | " | 75 " |
| R 6 | " -75R0A | " | 75 " |
| R 7 | " -82R0A | " | 82 " |
| R 8 | " -82R0A | " | 82 " |
| R 9 | " -75R0A | " | 75 " |
| CN 1 | SCV0511-40P | Connector | 40 Pin |
| S 1 | QSS2201-021 | Switch | |
| S 2 | " | " | |
| S 3 | " | " | |
| S 4 | " | " | |
| S 5 | " | " | |
| S 6 | " | " | |
| S 7 | " | " | |

## 6.7 BC BOARD

| Symbol No. | Part No. | Part Name | Description |
|---|---|---|---|
| S | QSS2201-021 | Switch | BACK COLOR |
| | SS30662-003 | Connector | 3 Pin |
| | " -012 | " | 12 Pin |